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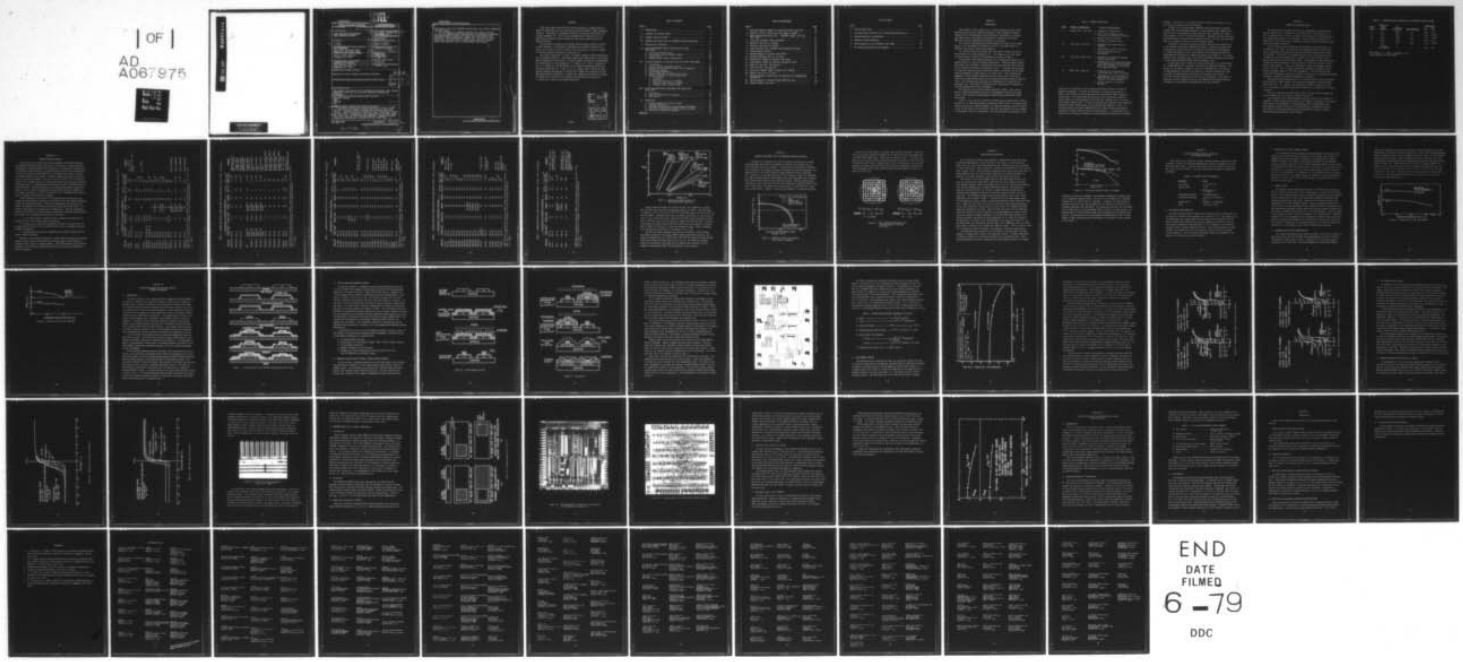

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Processing techniques for fabricating CMOS LSI arrays with 10^6 rads (Si) total-dose radiation hardness were developed under this contract. Radiation-hardened processes for these technologies include (1) bulk-silicon aluminum gate, (2) bulk-silicon silicon-gate closed CMOS logic (C^2L), and (3) silicon-gate CMOS/SOS. Megarad total-dose hardness was demonstrated on several LSIs with silicon-gate

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technologies, such as the CDP1802 microprocessor and an 8-bit arithmetic logic unit (ALU).

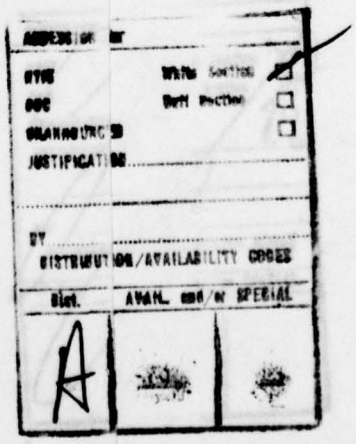
The total-dose and transient-radiation test results obtained with the ALU (TCS069) clearly demonstrated the advantages of combining radiation-hardened standard cell designs with radiation-hardened processing. These developments, funded under this contract, should dramatically increase the use of CMOS arrays in military weapons systems and spacecraft used in interplanetary explorations.

PREFACE

This final report describes the results achieved in a program directed toward the improvement of the total-dose radiation hardness of CMOS integrated circuits. The period of performance covered by this report was October 1973 through September 1977. The work was performed by RCA Corporation at the Solid State Technology Center, Somerville, New Jersey, under Contract No. N00014-74-C-0079.

The contract was funded by the Defense Nuclear Agency through the Office of Naval Research. We gratefully acknowledge the technical assistance and support of the Navy scientific officer for the program, Mr. Harold L. Hughes at the Naval Research Laboratory, Washington, DC.

The project leader was S. Cohen. H. Borkan, Manager of Custom Monolithics, was the project supervisor. Many other people also contributed to the achievements documented in this report. The author wishes particularly to acknowledge the contributions to this program of J. J. Fabula, D. S. Woo, S. Policastro, and C. D. Mulford for the development of the radiation-hardening process and for wafer fabrication; S. T. Hsu, A. Ipri, G. Hughes, and A. Feller for many helpful technical discussions; H. Hyman and N. Ciampa for assistance with the SEM radiation-test procedures; D. Clifton for assembly and electrical testing; D. Woronka and D. Brown for the radiation and reliability testing; and J. Corboy and J. Mack for the doped polysilicon.



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SECTION I

INTRODUCTION

The purpose of this contract was to conduct research directed toward improving the total-dose radiation hardness of CMOS integrated circuits. Whereas initial investigations involved hardness improvement of aluminum-gate CMOS arrays, later phases concentrated on hardening silicon-gate CMOS arrays on both sapphire and bulk-silicon substrates.

The research investigations performed under this contract were fundamental to the development and production by RCA of LSI CMOS arrays for satellite and nuclear radiation environments.

The contract effort was divided into four phases covering the period from October 1973 through September 1977. The objectives for each phase and their respective periods of performance are shown in Table 1.

During Phase I RCA studied techniques for ion-implanting aluminum into channel oxides for radiation-hardness enhancement. Channel-oxidation hardening studies were performed on experimental MOS capacitors processed with wet and dry oxides and varying concentrations of HCl. A technique was developed for using the scanning electron microscope (SEM) to determine the total-dose radiation hardness of CMOS arrays at the wafer level. This technique was suggested by Naval Research Laboratory and was used by RCA's Solid State Division for prescreening wafer lots for radiation-hardened satellite applications. The technology was published and disseminated for industrial and government use. The effects of different wafer metallization techniques on radiation hardness were also investigated.

The results of the various studies conducted in Phase I were used to define a radiation-hardened process for aluminum-gate, bulk-silicon, CMOS arrays. This process was demonstrated by fabricating megarad-hard CD4007-type arrays.

Phase II of the contract included a reliability and reproducibility demonstration of the radiation-hardened aluminum-gate CMOS process. As E-beam metallization was found to degrade hardness, an induction-melting system was adopted. A total of 300 arrays were delivered to NRL that were megarad hard and screened to MIL-STD-883, Class B, requirements. The major emphasis during Phase II was

TABLE 1. CONTRACT OBJECTIVES

Phase	Period of Performance	Areas of Investigation
I	October 1973 - July 1974	1. Aluminum ion implantation. 2. Use of the scanning-electron-microscope for hardness evaluation. 3. Channel oxidation studies. 4. Hardening of CD4007A arrays.
II	July 1974 - July 1975	1. Hardened-process demonstration (CD4024). 2. Metallization studies, IN-source. 3. Rad-hard CMOS/SOS process development.
III	July 1975 - April 1976	1. Continuation of CMOS/SOS rad-hard process development. 2. Demonstration of the rad-hard process by processing of an 8-bit arithmetic logic unit (TCS069) and fabrication of 30 rad-hard arrays.
IV	April 1976 - Sept 1977	1. Hardening of the bulk-silicon closed CMOS logic (C^2L) technology. 2. Investigation of the dependence of CMOS/SOS performance and radiation hardness on process parameters. 3. Process controls for hardness assurance.

placed on the translation of the radiation-hardening techniques to CMOS-on-sapphire technology. Initially the techniques for hardening developed in Phase I were applied to both silicon-gate and aluminum-gate CMOS-on-sapphire technologies. The Al-gate CMOS/SOS structures were comparatively simple to harden, since all high-temperature diffusions were completed prior to growing the hardened channel oxide. Because the aluminum-gate CMOS/SOS arrays exhibited threshold voltage instabilities, this technology was abandoned in favor of the self-aligned silicon-gate CMOS/SOS process, which offered the additional advantages of higher speed and greater packing density. Ion-implantation procedures were developed to eliminate the high-temperature diffusions that degrade

hardness. The effects of postchannel-oxidation thermal processing on total-dose radiation hardness were investigated.

In Phase III the silicon-gate, CMOS/SOS radiation-hardened technology evolved into a triple-implant process, in which separate boron implants were used for the P^+ source/drain and the polysilicon-gate regions, and a phosphorus implant for the N^+ source/drain regions. Megarad total-dose capability was demonstrated on a small-scale integrated circuit; 10^5-rad total-dose hardness, on a complex LSI array, an 8-bit arithmetic adder.

In Phase IV, attention was directed toward improving the producibility of the hardened silicon-gate CMOS/SOS technology. Alternate procedures for achieving more uniform polysilicon doping and thickness were investigated. A technique developed for the in situ doping of the polysilicon gates with boron improved producibility, radiation hardness, and stability. LSI arrays (TCS069, 8-bit arithmetic logic unit) were successfully fabricated and tested to total-dose radiation-hardness levels exceeding 1 Mrad.

An additional task of Phase IV was the modification of the bulk-silicon C^2L (Closed CMOS Logic) technology to increase its radiation hardness. The results of the previous (Phases II and III) investigations of the effects of high-temperature diffusions and anneals on radiation hardness were used to modify the standard RCA bulk-silicon, silicon-gate wafer process. A total-dose hardness capability of 500 krad, an improvement of two orders of magnitude over the commercial process, was demonstrated by fabricating and successfully testing RCA's microprocessor array (type CDP1802).

SECTION II

ALUMINUM ION IMPLANT STUDIES

The initial study was directed toward the development of procedures for the ion implantation of aluminum in the channel oxide. The purpose of the Al^+ ion implant was to prevent a buildup of space charge at the Al-SiO_2 interface under positive gate-bias irradiation. This is the bias condition that causes CMOS circuit failure due to excessive n-channel device threshold voltage shift under gamma irradiation.

The Al^+ implants were performed on two different ion accelerators: an Accelerators, Inc. model at the Solid State Technology Center in Somerville, and the experimental accelerator in the David Sarnoff Research Center (DSRC) in Princeton. Two sources of aluminum ions were tried, with varying success. A commercial (Al) hot-cathode source was found to be less efficient than a sputtered-aluminum source developed at DSRC. A procedure for angle implanting through the mass spectrometer at energy levels of 30-60 keV resulted in relatively stable implants. These were performed at effective energies ranging from 5 to 15 keV. Due to the low aluminum-ion currents, the implant time to achieve aluminum dosages of 10^{15} N/cm^2 averaged 8 h. RCA did not then have accelerators designed to provide the high-ion current at low accelerating voltages required to perform the efficient implanting of aluminum.

MOS capacitors were fabricated, on 1- to 2-Ω-cm, n-type silicon substrates with 850-Å, dry, 1000°C oxides. The oxides were implanted at various energy levels and doses. All implants were followed by a 600°C nitrogen anneal for 1 h. Capacitance-voltage-bias-temperature (CVBT) data for these runs are shown in Table 2.

The large, negative flatband voltage shifts for the 10.5-keV implants indicate penetration of the Si-SiO_2 interface by the Al^+.

The conclusions from these experiments and the results of Al^+ implant experiments of CMOS arrays indicated that the Al^+ implant techniques, to be viable, would require the development of accelerators capable of implanting at low accelerating voltages (5-10 keV) with high-efficiency aluminum-ion sources. This method for hardening CMOS arrays was abandoned when improved hardened channel-oxidation techniques were developed.

TABLE 2. ION-IMPLANT DATA OBTAINED WITH A SPUTTERED-ALUMINUM SOURCE

Implant Run	Effective Energy (keV)	Dose (ions/cm^2)	Time (minutes)	CVBT Data* V_{fb}	CVBT Data* ΔV_{fb}
K	6.5	10^{14}	20	+0.8	+1.0
M	8.5	10^{14}	45	+1.2	-2.6**
N	8.5	10^{15}	135	+2.4	-4.9**
P	10.5	10^{14}	15	+1.8	+1.0
Q	10.5	10^{15}	135	+3.4	-6.3**
-	Control (No implant)	-	-	+0.2	+0.6

*t = 5.0 min; T = 300°C; V (voltage) = 10 V.
**Data taken for 1 min at 300°C.

SECTION III

CHANNEL-OXIDATION STUDIES

Starting with the standard RCA channel-oxidation and anneal processes, an extensive investigation was conducted on the effects of channel-oxidation environments and postoxidation heat treatment on the radiation susceptibility of bulk-silicon MOS capacitors. Optimum radiation hardness was achieved with a clean, dry, undoped oxygen ambient for the channel-oxide growth, followed by a rapid quench to room ambient. Radiation hardness was found to vary inversely with oxide thickness. The use of dry O_2 at 1000°C for 2 h was established as the standard process for optimized radiation hardness and reliability. This growth time, at standard barometric pressure, results in 850-Å (typical) oxide thickness. Radiation hardness can be increased by growing thinner gate oxides, but at the cost of reducing both production yields and reliability. The thinner gate oxides ($\leq$700 Å), in particular, are considerably more susceptible to damage from electrical transients.

Table 3 summarizes the results of the experimental investigations performed with MOS capacitor structures to determine the optimum channel-oxidation process for radiation hardness. The initial experiments with growing hard oxides concentrated on the effects of HCl used during the growth cycle. The hardness decreased with increasing HCl concentrations. The next experiments dealt with the effects of various anneal treatments on radiation susceptibility. The results can be summarized very briefly, as follows:

1. If the oxide had been quenched rapidly, radiation hardness was not enhanced by any of the anneal cycles investigated.

2. The Q_{ss} can be reduced by an appropriate anneal, but great care must be exercised in the choice of the anneal cycle so as not to degrade radiation hardness excessively.

3. Postoxidation processing at temperature above 900°C substantially degrades radiation hardness.

Analysis of the radiation behavior of the MOS capacitors shows some general trends. Figure 1 plots the flatband shift versus dosage of MOS capacitors irradiated with a positive voltage (stress: $+10^6$ V/cm) applied to the aluminum electrode. All oxides were between 850 and 950 Å, and metal was deposited by E-beam techniques.

TABLE 3. CHANNEL-OXIDATION INVESTIGATIONS (MOS CAPACITORS, N-TYPE, [100]

Exp. No.	Description of Oxidation Technique: Oxide Type*	Growth Time	Anneal	Implant	Initial V_{fb} ($-V^{\dagger}$)	Total Dose** [rads (Si)]	Comments
4255N	Dry O_2	3 h	No	No	0.8	10^5	t_{ox} = 1113 Å
SC-206	1% HCl-dry O_2	100 min		No	0.3	$>10^5$	Incorrect dose rate on SEM
203-N	Dry O_2	100 min		Yes	0.6	10^5	
203-Q	Dry O_2	100 min		Yes	0.6	2×10^5	
	Dry O_2	3 h	No	No	0	5×10^5	t_{ox} = 1040 Å
SC-108		100 min		No	0.1	10^4	
EXP-001-2	5% HCl-dry O_2	90 min		Yes	1.2	10^4	
EXP-001-3	5% HCl-dry O_2	90 min		Yes	1.3	3×10^4	
SC-110	Dry O_2	2 h	No	No	0.1	10^6	
SC-110	Dry O_2	2 h	FG-1100°C	No	0	5×10^4	
SC-115-B	Dry O_2	2 h	No	No	0	$>10^6$	
SC-115-A	Dry O_2	2 h	FG-1100°C	No	0.3	3×10^4	
SC-113-9	Dry O_2	2 h	FG-1100°C	No	0	6×10^4	
SC-113-10	Dry O_2	2 h	No	No	0	10^6	
SC-117	Dry O_2	100 min	No	No	0.3	10^6	
TCE-012-1	Dry O_2	2 h	He-1000°C 20 min	No	0	10^6	E-gun (aluminum)
TCE-012-3	Dry O_2	2 h	FG-1100°C 20 min	No	0.2	6×10^4	E-gun (aluminum)
TCE-012-2	Dry O_2	2 h	FG-1000°C 20 min	No	0	2×10^5	E-gun (aluminum)
TCE-012-9	Dry O_2	2 h	No	No	0.2	10^6	E-gun (aluminum)

*All the dry O_2 oxides were grown at 1000°C; unless otherwise noted, O_2 flow was 2 L/min.

**For ΔV_{fb} = 2 volts (V); V (voltage) = 10 volts (V) during irradiation.

†-V = -volts.

TABLE 3. CHANNEL-OXIDATION INVESTIGATIONS (MOS CAPACITORS, N-TYPE, [100] (Continued)

Exp. No.	Description of Oxidation Technique: Oxide Type*	Growth Time	Anneal	Implant	Initial V_{fb} (-V†)	Total Dose** [rads (Si)]	Comments
TCE-012-10	Dry O_2	2 h	No	No	0	8×10^5	Postmetal alloy - 500°C, 10 min FG
TCE-012-11	Dry O_2	2 h	No	No	0.5	3×10^5	Filament metal, standard alloy
TCE-012-12	Dry O_2	2 h	No	No	0.2	3×10^5	Filament metal postmetal alloy - 500°C, 10 min
#24	875°C HCl steam	45 min	FG-1100°C 20 min	No	1.0	3×10^4	Filament metal, standard alloy
TCE-013-1	875°C HCl steam	45 min	FG-1100°C 20 min	No	0	6×10^4	E-gun (standard alloy)
TCE-013-2	875°C HCl steam	45 min	FG-1000°C 20 min	No	0	2×10^5	E-gun (standard alloy)
TCE-013-3	875°C HCl steam	45 min	He-1000°C 20 min	No	0	2×10^5	E-gun (standard alloy)
TCE-014-A	Dry O_2	2 h	No	No	0	10^6	Filament metal, 450°C; FG alloy, 45 min
TCE-014-B	Dry O_2	2 h	No	No	0	10^6	Filament metal, 450°C; FG alloy, 25 min
TCE-014-C	Dry O_2	2 h	No	No	0	10^6	Filament metal, 500°C; FG alloy, 25 min
TCE-014-D	Dry O_2	2 h	No	No	0	10^6	Filament metal, 500°C; FG alloy, 10 min
TCE-015	Dry O_2	2 h	No	No	0.3	10^6	1-2 Ω-cm <1-0-0>
TCE-015	Dry O_2	2 h	No	No	0.6	3×10^5	3-5 Ω-cm <1-1> (PMOS wafer material)

*All the dry O_2 oxides were grown at 1000°C; unless otherwise noted, O_2 flow was 2 L/min.
**For ΔV_{fb} = 2 volts (V); V (voltage) = 10 volts (V) during irradiation.
†-V = -volts.

TABLE 3. CHANNEL-OXIDATION INVESTIGATIONS (MOS CAPACITORS, N-TYPE, [100] (Continued)

Exp. No.	Description of Oxidation Technique: Oxide Type*	Growth Time	Anneal	Implant	Initial V_{fb} ($-V^{\dagger}$)	Total Dose** [rads (Si)]	Comments
SC-120B	Dry O_2	2 h	No	No	0	10^6	
SC-120A	Dry O_2	4 h	No	No	0	3×10^5	
SC-122	Dry O_2	2 h	No	No	0.1	10^6	
SC-123	Dry O_2	3 h	No	No	0.5	3×10^5	
SC-127	Dry O_2	90 min	No	No	0.2	10^6	
SC-130	Dry O_2	2 1/4 h	No	No	0.6	3×10^5	
SC-129	Dry O_2	1 3/4 h	No	No	0.2	10^6	
SC-131	Dry O_2	2 h	No	No	0	$>10^6$	Shift of -3 volts at 5×10^6 rads (Si)
SC-133	Dry O_2	2 h	No	No	0.1	10^6	
SC-134	Dry O_2	3 h	No	No	0.6	2×10^5	
SC-135	Dry O_2	145 min	No	No	0.3	5×10^5	Filament metal
SC-136	Dry O_2	3 h	No	No	0.3	2×10^5	
SC-139-1	Dry O_2	2 h	No	No	0.2	8×10^5	Filament metal
SC-139-2	Dry O_2	2 h	No	No	0.3	10^6	E-gun metal
SC-140-1	Dry O_2	3 h	No	No	0.2	6×10^5	Filament metal
SC-140-2	Dry O_2	3 h	No	No	0.3	6×10^5	E-gun metal
SC-141-1	Dry O_2	4 h	No	No	0.3	2×10^5	Filament metal
SC-141-2	Dry O_2	4 h	No	No	0.4	2×10^5	E-gun metal
E-256	Dry O_2	2 h	No	No	0.1	10^6	
SC-131 Repeat	Dry O_2	2 h	No	No	0.4	$>10^6$	Metal E-gun
TCE-017	Dry O_2	2 h	No	No	0.5	10^6	Filament metal (3-5 Ω-cm)

*All the dry O_2 oxides were grown at 1000°C; unless otherwise noted, O_2 flow was 2 L/min.
**For ΔV_{fb} = 2 volts (V); V (voltage) = 10 volts (V) during irradiation.
†-V = -volts.

TABLE 3. CHANNEL-OXIDATION INVESTIGATIONS (MOS CAPACITORS, N-TYPE, [100] (Continued)

Exp. No.	Description of Oxidation Technique: Oxide Type*	Growth Time	Anneal	Implant	Initial V_{fb} ($-V^{\dagger}$)	Total Dose** [rads (Si)]	Comments
SC-144	Dry O_2	2 h	No	No	0.3	3×10^5	Metal E-gun
SC-146	Dry O_2	2 h	No	No	0.2	10^6	Filament metal
TCE-017-2	Dry O_2	2 h	No	No	0.2	2×10^5	1-2 Ω-cm
TCE-019	Dry O_2	2 h	No	No	0.3	7×10^5	
TCE-019	Dry O_2	2 h	No	No	0.4	3×10^5	
TCE-019	Dry O_2	2 h	No	No	0.2	10^6	
TCE-019	Dry O_2	2 h	No	No	0.2	10^6	
TCE-019	Dry O_2	2 h	No	No	0.6	5×10^5	
TCE-017A	Dry O_2	2 h	He-1000°C	No	0.3	3×10^5	
TCE-017B	Dry O_2	2 h	He-900°C	No	0.4	8×10^5	
TCE-017C	Dry O_2	2 h	He-800°C	No	0.4	5×10^5	
TCE-017D	Dry O_2	2 h	He-700°C	No	0.3	2×10^5	
TCE-017E	Dry O_2	2 h	He-600°C	No	0.7	3×10^5	
SC-147	0.5% HCl, dry O_2	2 h	No	No	0.4	2×10^5	4 L/min O_2 flow
SC-148	Dry O_2	2 h	No	No	0.5	4×10^5	4 L/min O_2 flow (No sinter)
SC-148	Dry O_2	2 h	No	No	0.5	10^6	
SC-149	Dry O_2	2 h	No	No	0.5	$>10^5$	
SC-150	Dry O_2	2 h	No	No	1.5	10^5	Slow pull
SC-151	Dry O_2	2 h	No	No	0.5	3×10^5	Slow pull
SC-152	Dry O_2	2 h	No	No	0.3	10^6	Quench pull with lot #247

*All the dry O_2 oxides were grown at 1000°C; unless otherwise noted, O_2 flow was 2 L/min.

**For ΔV_{fb} = 2 volts (V); V (voltage) = 10 volts (V) during irradiation.

$^{\dagger}-V$ = -volts.

TABLE 3. CHANNEL-OXIDATION INVESTIGATIONS (MOS CAPACITORS, N-TYPE, [100] (Continued)

	Description of Oxidation Technique						
Exp. No.	Oxide Type*	Growth Time	Anneal	Implant	Inital V_{fb} (-V†)	Total Dose** [rads (Si)]	Comments
SC-153	Dry O_2	2 h	No	No	1.2	5×10^5	2.5 L/min - slow pull
7A-A	Dry O_2	2 h	No	No	0.2	$>10^6$	Flatband shift of -1.1 volt at 10^6 rads (Si)
7A-B	Dry O_2	2 h	He-1000°C 30 min	No	0.3	3×10^5	
7A-C	Dry O_2	2 h	He-900°C	No	0.3	$>10^6$	Flatband shift of -1.7 volt at 10^6 rads (Si)
7A-D	Dry O_2	2 h	He-800°C	No	5.8	$>10^6$	Flatband shift of -1.5 volt at 10^6 rads (Si) (probably wet oxide tube)

*All the dry O_2 oxides were grown at 1000°C; unless otherwise noted, O_2 flow was 2 L/min.
**For ΔV_{fb} = 2 volts (V); V (voltage) = 10 volts (V) during irradiation.
†-V = -volts.

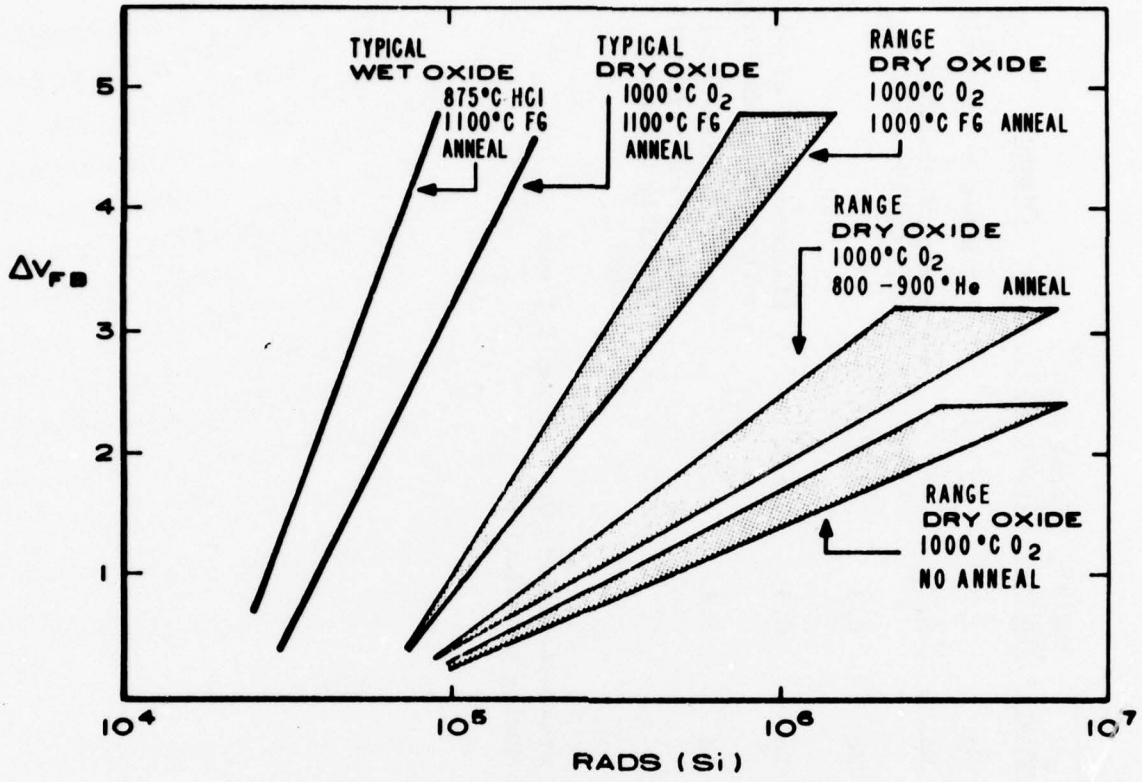

Figure 1. *Radiation-hardness summary for* bulk-silicon MOS capacitors.

Typical plots are shown for an 875°C wet HCl and a 1000°C dry O_2 oxide, both of which were annealed in forming gas (H_2/N_2) at 1100°C. The difference in hardness, for V_{fb} = 2 volts (3.8×10^4 for the HCl oxide versus 6.0×10^4 for the dry oxide), is normally seen and is probably attributable to the incorporation of Cl_2 in the 875°C oxide. Note that the 1100°C anneal destroys the hardness of the dry oxide, but still leaves it harder than the HCl oxide. The next group shows the range of many 1000°C dry oxides that were annealed in forming gas at 1000°C in an attempt to lower the flatband voltage. Typical hardness, still dominated by the effect of the anneal, is 2.0×10^5.

The last two groups represent the results of testing of "hard" oxides. The hardest oxides are the dry-O_2, 1000°C oxides grown without anneal. They range in hardness from 1.5×10^6 to 3.5×10^6 rads (Si) and can be reproducibly grown with flatband voltages from -0.3 to -0.6 V. The 1000°C dry undoped oxide, with no anneal, was adopted as the standard gate insulator for the hardened, aluminum-gate CMOS arrays developed on this contract.

SECTION IV

HARDNESS MONITORING WITH THE SCANNING-ELECTRON MICROSCOPE

A technique for sampling wafer runs for radiation hardness was successfully developed and used for all hardness testing on the contract until a cobalt-60 gamma source was acquired. A paper based on this effort, entitled "SEM Irradiation for Hardness Assurance Screening and Process Definition," was presented at the 1974 IEEE Nuclear and Space Radiation Effects Conference [1]. Dosimetry for the SEM irradiation of MOS capacitors (bulk Si); CMOS/SOS, bulk CMOS processed wafers; and packaged arrays was established and correlated with cobalt-60 and 1-MeV electron radiation sources. Typical electron-beam voltages used are 32 keV for metal-gate MOS capacitors, 37 keV for bulk-silicon, and 47 keV for SOS. The beam current density was 5.3×10^9 A/cm^2 for a dose rate of 5000 rads/s. Figure 2 illustrates the degree of correlation achieved.

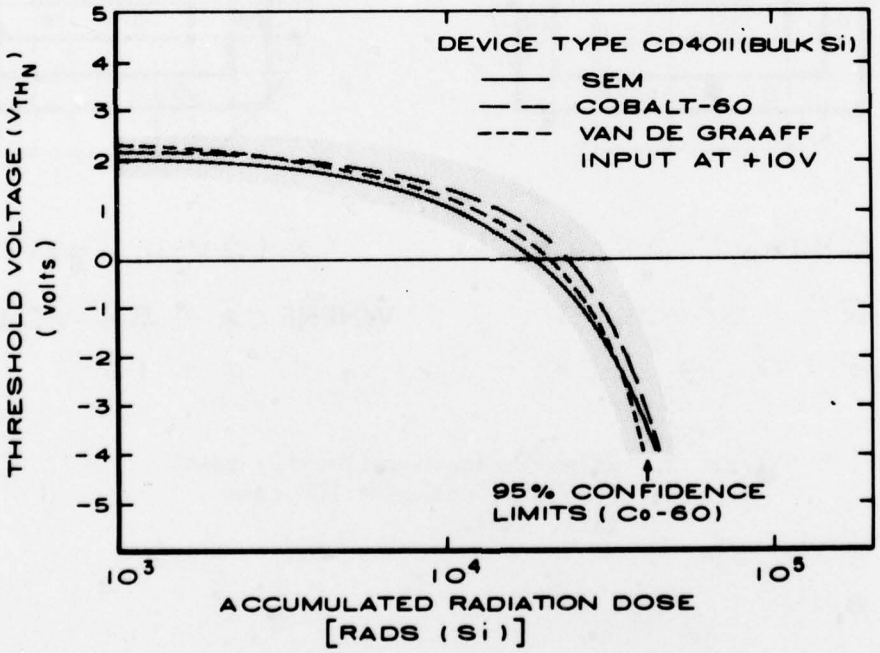

Figure 2. Radiation effects correlation study (V_{TH_N} vs dosage).

A dose rate of 5000 rads/s is normally used for SEM irradiation. The variance in total-dose radiation hardness over a single wafer was investigated for a hardened CMOS CD4007 array. These data are shown in Fig. 3. The wafer map data for the 19 pellets tested indicated that the variances for both the N- and P-transistors were within 2 sigma limits for 95% of the devices. The hardness sampling techniques developed during this study were employed successfully on other programs by RCA's Solid State Division, and disseminated to other companies for their use.

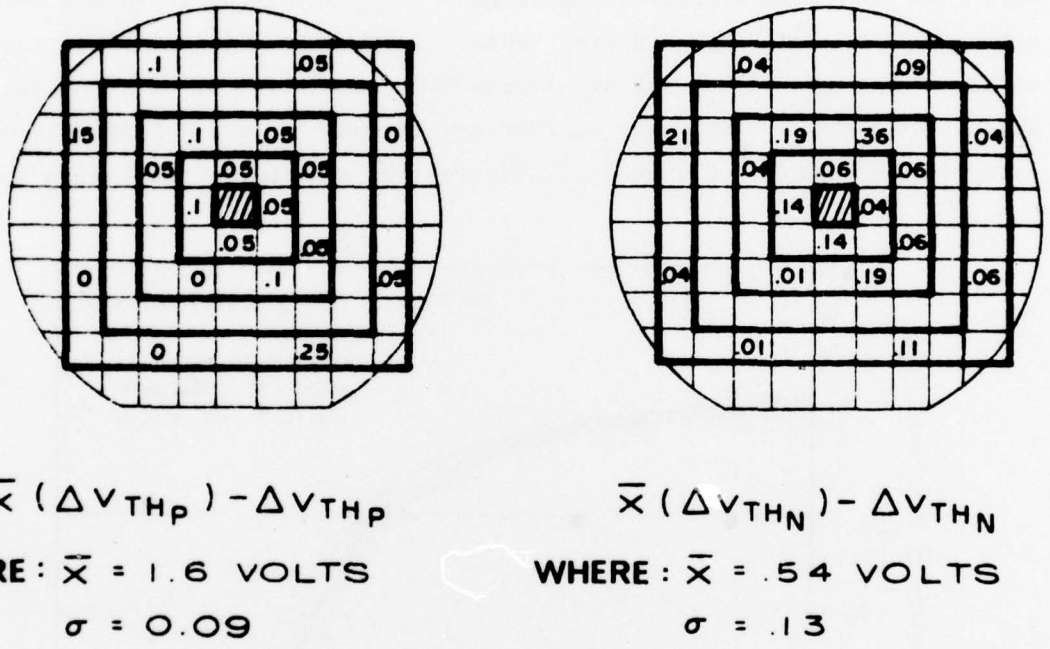

Figure 3. Wafer hardness-uniformity test. [CD4007A; dosage = 10^6 rads (Si), SEM].

SECTION V

METALLIZATION TECHNIQUES

The techniques for depositing aluminum on hardened MOS arrays were under continuous investigation over the period of the contract. During the first phase, when the bulk of the hardening effort was concentrated on the processing of metal-oxide-silicon (MOS) capacitors, aluminum was evaporated with an electron-beam (E-beam) system. When hardened aluminum-gate CMOS arrays were fabricated, it became apparent that the electron-beam evaporation of aluminum degraded the hardness of the PMOS transistors under positive gate-bias conditions.

The effects of the oxide damage caused by the high-energy (10 keV) electrons in the E-gun were evaluated by splitting two lots of arrays processed with hardened channel oxides, metallizing half the lot by electron-beam evaporation and the remainder with filament-evaporated aluminum. The metal-alloy cycle was identical (450°C, N_2, 15 min). Samples from each metallization technique were packaged and tested to total-dose radiation levels up to 10^6 rads (Si). The threshold voltage shifts were plotted for both N- and P-type transistors and are shown in Fig. 4. The effects of the oxide damage caused by the E-beam are clearly evident at total-dose radiation levels beyond 10^5 rads (Si). Below 10^5 rads, where the effects of positive oxide charge predominate, the N- and P-transistor voltage shifts for both E-gun- and filament-processed wafers are essentially the same. Above 10^5 rads the effects of the additional interface states in the oxide caused by the E-beam damage are clearly evident. Since the interface charge compensates for the positive-charge buildup at the $Si-SiO_2$ interface, the effect on the N-transistor is to reduce the threshold voltage shift, as evident in the "flattening" of the ΔV_{TH_N} curve (Fig. 4). On the other hand, with increasing radiation dose, the P-transistor curve for E-gun metal shows a monotonic shift toward more negative values. The net effect is that the P-transistor-threshold voltage is increased on E-beam metallized samples.

The experiment was repeated on one lot (#291) of another CMOS array type, CD4024, a 7-stage binary counter, with identical results. Filament evaporation of metal was adopted as an interim procedure for all hardened arrays. While this metallization technique eliminated the E-beam damage problem, the filament

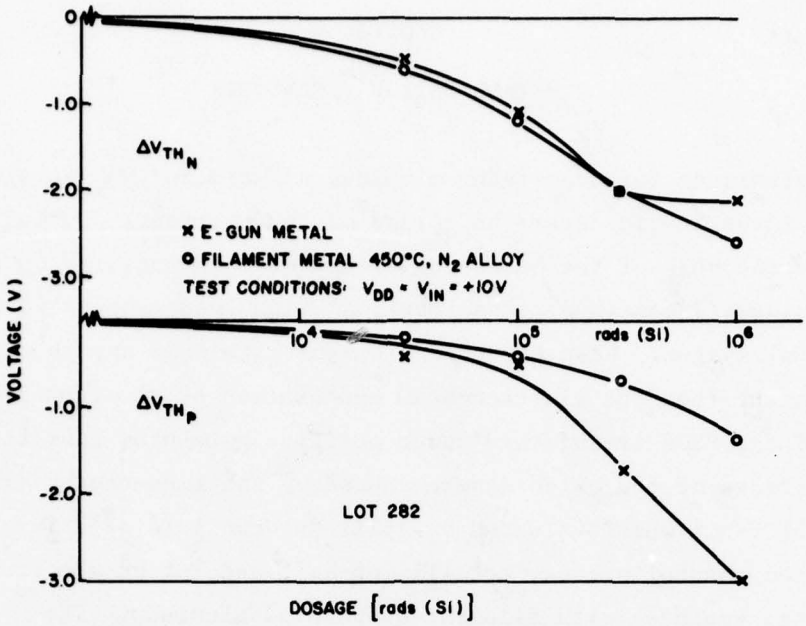

Figure 4. Total-dose hardness; E-gun vs filament.

evaporation system was incapable of reproducibly providing low sodium levels in the evaporated aluminum films. The source of the sodium is the tungsten filament that is used to melt the aluminum. In Phase II of the contract an rf-heated crucible source was purchased for the program, and procedures for aluminum evaporation were developed. The system was used also for the single-source evaporation of silicon-aluminum films in Phase IV of the contract, for metallization of the silicon-gate CMOS arrays processed on bulk-silicon substrates. The discussion of the development and application of the rf source (Model IN-1500, Applied Materials Corporation) is included in later sections of this report.

SECTION VI

RADIATION-HARDENED PROCESS DEFINITION OF Al-GATE CMOS ARRAYS

The results of the oxidation, anneal, and metallization studies were used to define a process for achieving megarad-hard total-dose capability for aluminum-gate CMOS arrays. The radiation-hardened process parameters centered on the values listed in Table 4. All other processing conformed to standard RCA procedures.

TABLE 4. RAD-HARD PROCESS PARAMETERS

Procedure	Value
Well Doping	6.0×10^{16} cm^{-3}
Channel Oxide	750 Å
	90-min, dry O_2; t = 1000°C
Postoxidation Anneal	No anneal-quench
Source-drain Spacing	7.5-8.75 μm (0.30-0.35 mil)
Metallization	Filament or rf melting
Alloy	450°C, N_2, 15 min

A. WELL-DOPING CONSIDERATIONS

To prevent depletion-mode n-channel device operation after irradiation, the N-transistor threshold voltage needed to be raised to 2.0 V. The higher Q_{ss} of the unannealed, dry channel oxide and the thinner (than standard HCl-steam grown) channel oxide required for radiation hardness effectively reduce the N-transistor threshold by approximately 0.5 V, as compared to the threshold voltage of RCA's standard commercial process. The 2.0-V threshold was accomplished by increasing the boron concentration in the p-well of the n-type silicon substrate. The P-transistor threshold voltage is determined by the resistivity of the n-type silicon substrate.

B. SOURCE-DRAIN SPACING (CHANNEL LENGTH)

The "as-defined" channel length of the aluminum-gate CMOS process is decreased by the additional lateral diffusion of the dopant species (boron or phosphorus) that occurs during the growth of the hardened gate insulator (1000°C, 90-minute, dry oxide). This lateral diffusion for the rad-hard process is greater than that for the standard oxidation (875°C, 45 min), which is followed by an 1100°C short-time anneal. The effect of the greater lateral diffusion is to decrease the source/drain punch-through voltage of both the N- and the P-transistors. To compensate for the increased lateral diffusion, the specification for the channel length as defined by the gate photomask was modified to 7.5-8.75 μm (0.30-0.35 mil) instead of the 6.25-8.75 μm (0.25-0.35 mil) normally used.

C. CHANNEL OXIDE

The channel-oxide thickness was specified at 750 Å, with a tolerance of ±50 Å. Since the growth rate of dry, undoped oxide is a function of moisture content of the oxygen source as well as atmospheric pressure, the gas supplies to the furnaces were filtered, and condensables removed by passing the gas through liquid-nitrogen cold traps. Special care was taken to ensure the cleanliness of the dry-oxidation furnace. This is necessary because no HCl can be used for soldium gettering in the extended (90 min) dry-oxidation cycle. The furnaces were equipped with HCl generators and were cleaned overnight with HCl steam (at 1000°C), then purged for 1 h with dry nitrogen to ensure removal of all moisture and HCl, prior to the growth of the channel oxide. Subsequent studies [2] of the reproducibility of hardened, dry channel oxides processed without recleaning and purging of the furnace after each run were performed. They showed no degradation of radiation hardness for at least six consecutive oxidation runs, equivalent to more than one single-shift operation.

D. HARDENED-ARRAY PROCESS DEMONSTRATION

The radiation-hardened process defined in Table 4 was used to process two CMOS array types, RCA types CD4007A (dual-complementary pair plus inverter), and CD4024A (7-stage binary counter) to demonstrate a total-dose hardness capability of 10^6 rads (Si). Two-hundred CD4007A and one-hundred CD4024A

arrays were packaged and screened in accordance with MIL-STD-883, Method 5004 requirements for Class B microelectron circuits. Typical SEM radiation-hardness curves are shown in Fig. 5 for the CD4007A array and in Fig. 6 for the CD4024A. These hardness curves were taken for "worst-case" test conditions since the postradiation electrical tests were performed within seconds after the electron beam was turned off. Subsequent radiation testing of packaged CD4007A and CD4024A arrays by government laboratories confirmed that the arrays met functional requirements after exposure to a total dose of 10^6 rads (Si) of gamma irradiation. The yield to the MIL-STD-883 screening procedures (Method 5004, Class B) for these radiation-hardened arrays was equivalent to yields for standard-processed CMOS arrays.

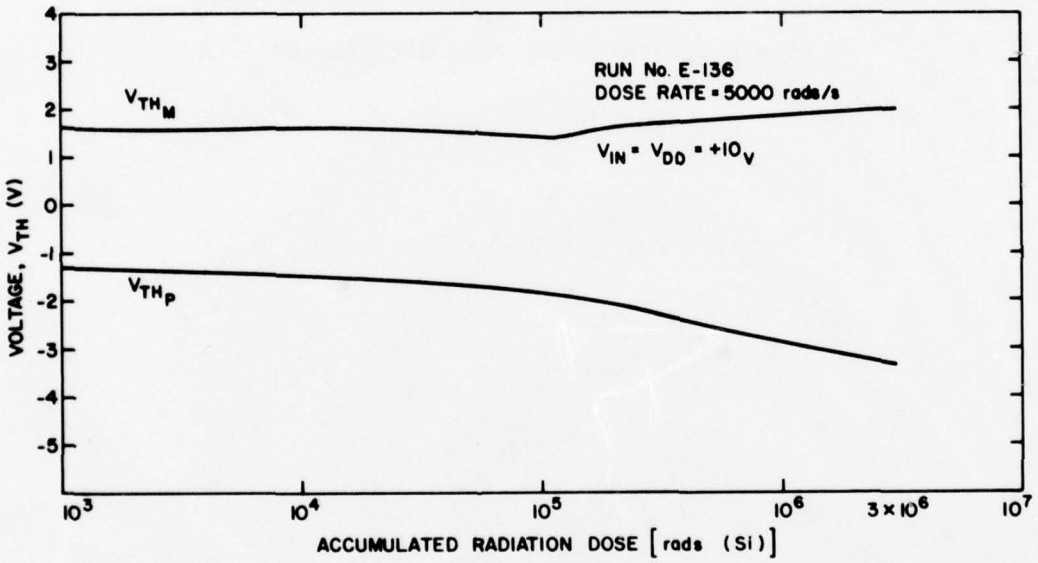

Figure 5. Radiation test data for CD4007A.

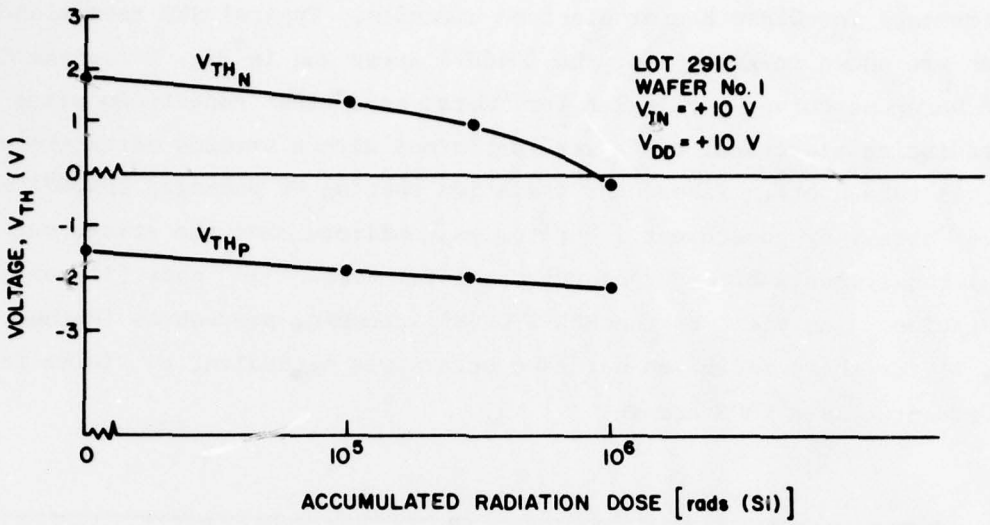

Figure 6. Radiation test data for CD4024A.

SECTION VII

RADIATION-HARDENED SILICON-GATE CMOS/SOS PROCESS DEVELOPMENT

A. INTRODUCTION

The major portion of the contractual effort centered on the development of processes for improving the total-dose hardness of CMOS arrays on sapphire. CMOS/SOS offers a number of enhanced characteristics over bulk-silicon CMOS. The sapphire serves as an inert substrate and provides a suitable crystal lattice upon which the silicon is grown epitaxially. Since dielectric isolation is provided by the sapphire, and the diffusions terminate the sapphire wafers, unwanted circuit capacitance is minimized. This significantly increases the speed, reduces dynamic power consumption, and enhances transient radiation hardness. In addition, since isolation regions are inherent, the packing density of SOS becomes greater than that for conventional bulk-silicon CMOS, which requires guard bands or oxide isolation. Even greater packing density and higher speed are achieved by use of self-aligned silicon-gate technology, which eliminates the overlap capacitance inherent in the metal-gate process.

In this process the polysilicon gate is deposited immediately after the gate oxide is grown. The polysilicon protects the gate oxide during all subsequent processing, resulting in enhanced device stability. The advantages of greater packing density, higher speed, and enhanced stability afforded by the self-aligned silicon-gate technology mandated its use for radiation-hardened process development.

The silicon-gate CMOS/SOS process developed at RCA Laboratories was transferred to the Solid State Technology Center (SSTC) and optimized for LSI array fabrication under an Air Force Manufacturing Methods Program (F33615-73-C-5043). Both the double-epitaxial and single-epitaxial ion-implanted process, each utilizing diffused P^+ polysilicon gates, were defined by RCA under this contract. The double-epitaxial process, providing independent control of the NMOS and PMOS transistor thresholds, was selected for the fabrication of radiation-hardened CMOS/SOS arrays. A cross-sectional view of the double-epitaxial process is shown in Fig. 7. The enhancement-mode NMOS and PMOS transistors were fabricated on 0.6-μm-thick epitaxial islands of p-type and n-type single crystalline silicon films deposited on a sapphire wafer.

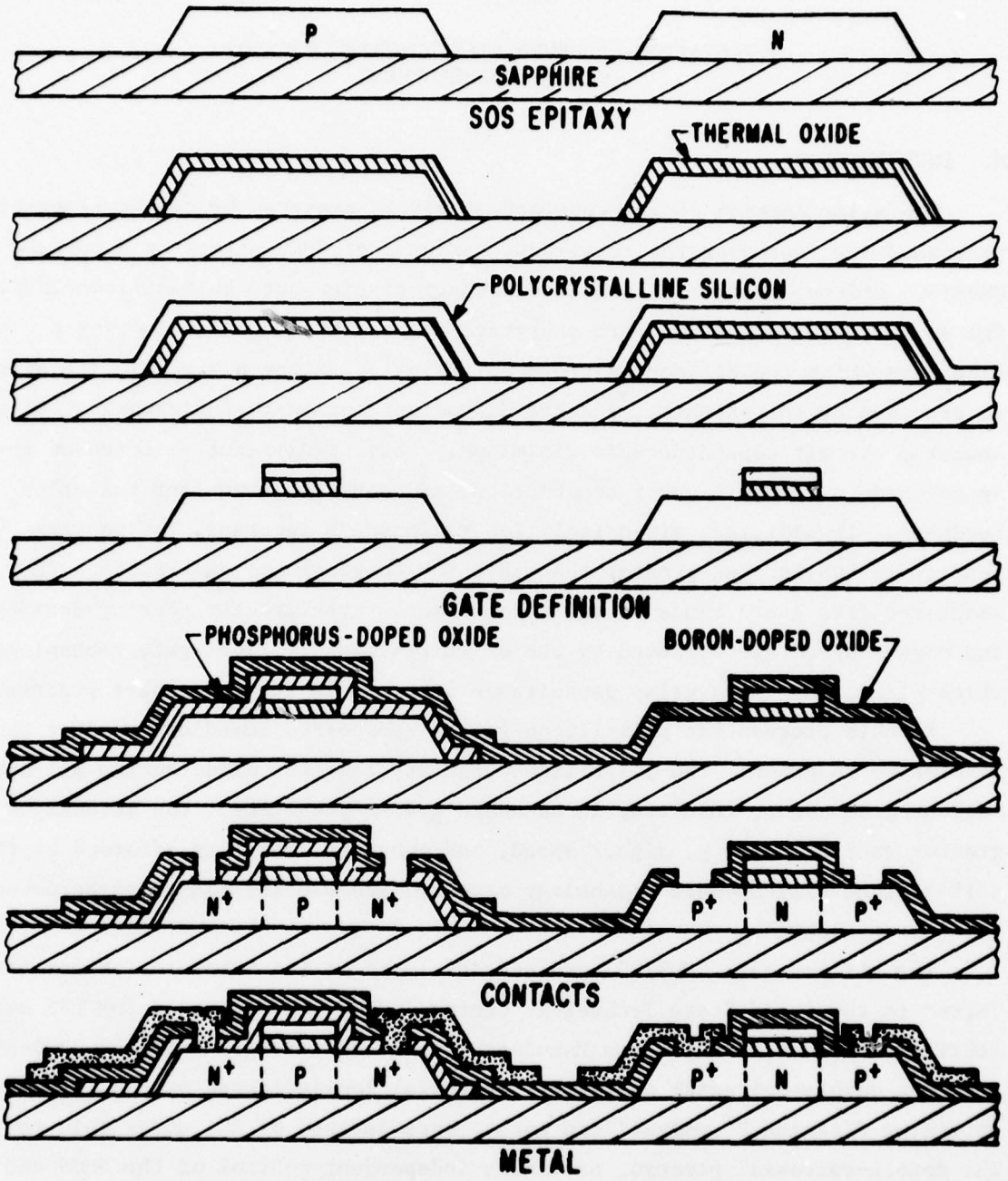

Figure 7. Cross-sectional view, RCA/SSTC double-epitaxial process.

B. INITIAL RADIATION-HARDENING EFFORTS

The initial approach to hardening the silicon-gate CMOS/SOS process was to use the 1000°C "dry" undoped oxide instead of the 940°C HCl steam normally employed for the gate dielectric. While the MOS bulk-silicon capacitor controls processed with the 1000°C, 750-Å oxide exhibited flatband shifts of less than 2.0 V after a 10^6-rad total dose, the devices processed with this gate insulator exhibited only slightly improved (10^4 rads) radiation tolerance. Additional runs were processed with dry oxide and reduced diffusion temperatures and times. The normal 1050°C diffusion temperature for doping the polysilicon gate and source/drain regions was reduced to 950°C. This increased polysilicon resistivity and decreased junction depths, but did not enhance radiation hardness. The next approach was to eliminate the high-temperature diffusions by the use of ion-implantation techniques with reduced drive-in and anneal temperatures. RCA Laboratories had developed a silicon-gate CMOS/SOS process based on ion-implantation techniques. This technology, modified by incorporation of the hardened channel dielectric, resulted in the first megarad-hard CMOS/SOS process demonstration.

A cross-sectional view of the triple-implant procedure is shown in Fig. 8. The sequence of the radiation-hardened process development, starting with the triple-implant technology, is outlined below.

- The Triple-Implant Process.
- Investigation of Back-Channel Leakage ("Wet" vs "Dry" Channel Oxides).
- In situ-Doped Polysilicon.
- Implant Procedures for LSI Circuits.
- Hardened LSI Process Demonstration with the TCS059 test chip and the TCS069 8-bit arithmetic arrays.

C. HARDENED Si-GATE CMOS/SOS ARRAYS (TRIPLE IMPLANT PROCESS)

In this process, enhancement-mode devices were fabricated on 0.6-μm-thick epitaxial-silicon islands of p- and n-type single-crystal silicon films on a sapphire wafer. The epi-islands are provided by a two-step hetero-epitaxial process [see Technical Report AFML-1R-516-3 (3)]. The gate oxide for the initial runs consisted of an undoped, 750±50-Å-thick silicon dioxide layer

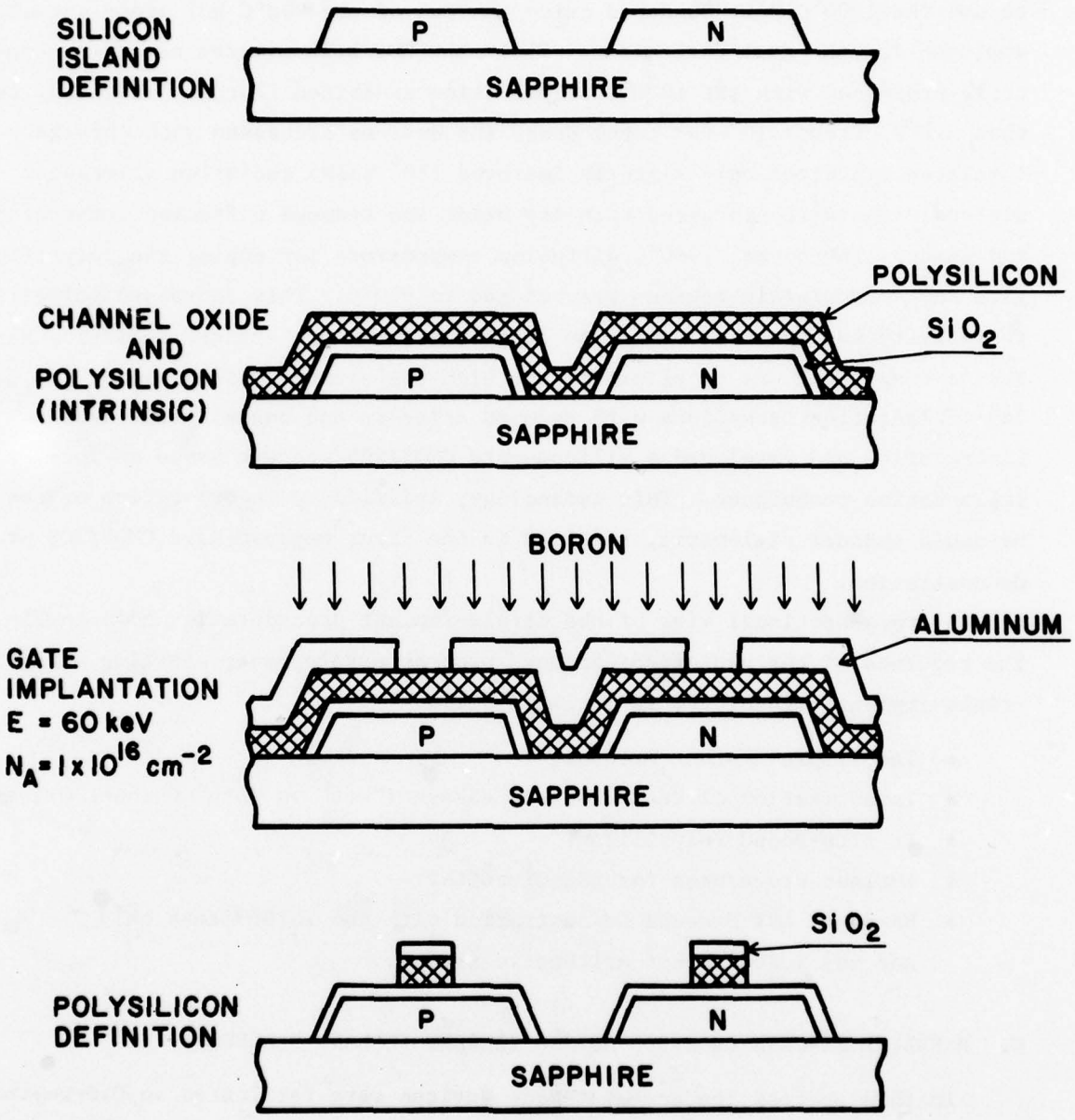

Figure 8. Triple-implant process.

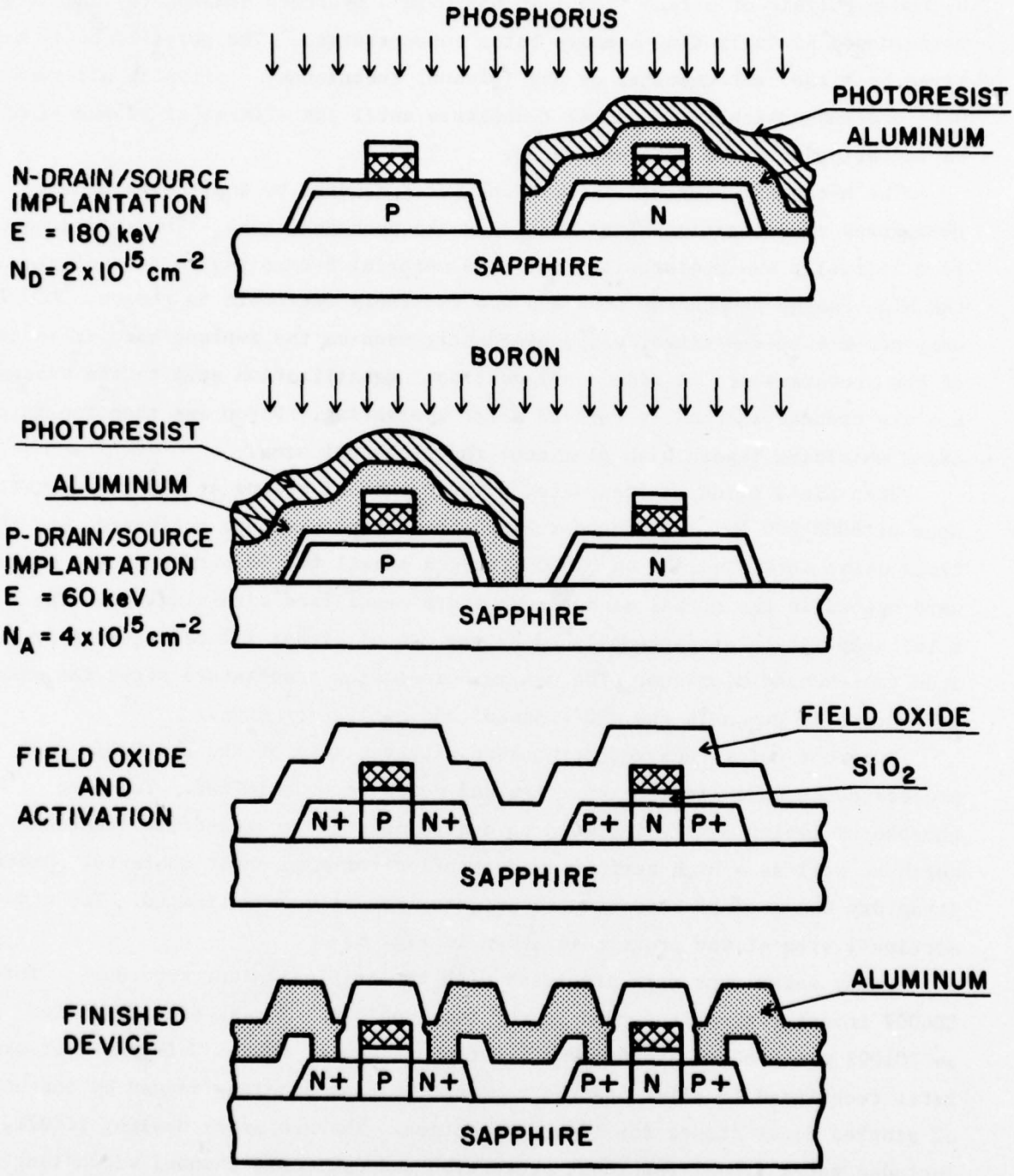

Figure 8. (Continued).

grown at 1000°C with dry O_2. The polysilicon gate was then deposited, undoped, by the pyrolysis of silane (SiH_4) at 650°C in a hydrogen atmosphere, and afterwards doped by implanting a heavy boron concentration. The polysilicon is defined by either wet chemical or dry (plasma) techniques. Initially all runs were processed with wet chemical techniques until the effects of plasma etching on radiation hardness were evaluated.

The n-channel source/drain regions were prepared by implanting a heavy phosphorus concentration after shielding the p-channel area. The shielding film initially was photoresist, but this material became highly polymerized by the high-energy phosphorus ions and was extremely difficult to remove. Aluminum, non-E-beam-deposited, was subsequently used as the implant barrier instead of the photoresist. It added one additional metallization step to the process, but was cleaner and easily removed after implanting. Boron was then implanted after shielding (again with aluminum) the n-channel area.

Then field oxide was deposited by pyrolysis of silane at 450°C to a thickness of 6000 ± 500 Å. The phosphorus and boron implants were activated, and the field oxide densified, by an 850°C nitrogen anneal for 90 minutes. The contacts were opened in the normal manner and wafers metallized with aluminum. The metal evaporation was accomplished by the use of either filament-heated or induction-heated aluminum. The maximum processing temperature after the gate dielectric is grown is the 850°C anneal and activation step.

Numerous wafer runs were processed with variants of the triple-implant process described. Implant energies and doses were optimized. Two-step phosphorus implants were included to ensure adequate source-drain junction depth as well as a high surface concentration for good ohmic contacts. Other (than dry O_2) channel oxidation techniques were also investigated. The cross-sectional view of the process is shown in Fig. 8.

Other wafer runs were processed with the triple-implant procedure. The CD4007 inverter circuit served as the test vehicle. A mask set identified as TC1092 was used to process the first experimental runs. This mask set was later redesigned to eliminate the terminal leakage problems caused by the use of stacked Zener diodes for input protection. The new array design, TCS071, included gated diodes for input protection and optimized channel width/length ratios for the N- and P-transistors. A microphotograph of the TCS071 is shown in Fig. 9.

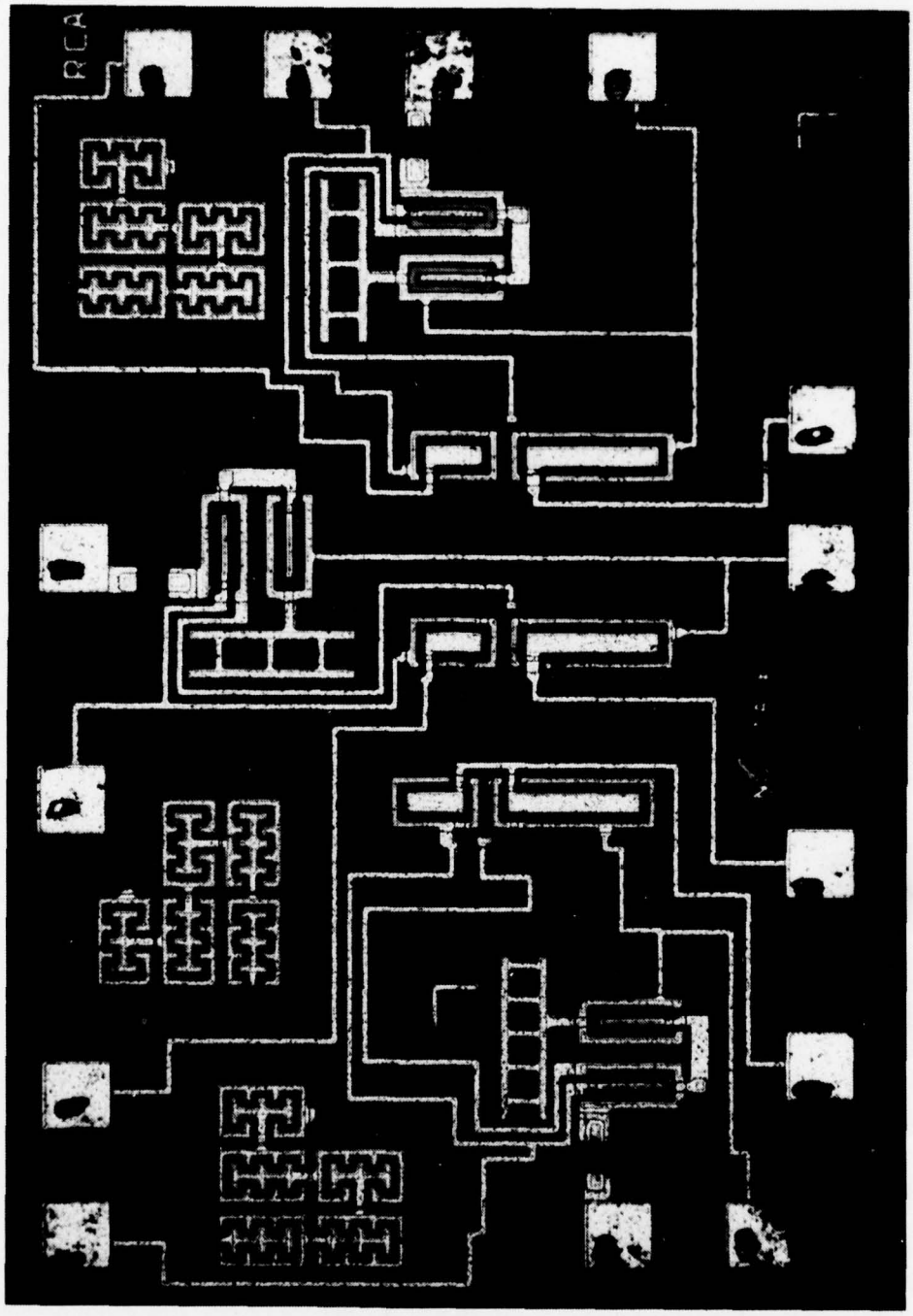

Figure 9. Microphotograph of inverter array TCS071.

Lot S280, processed with implanted polysilicon gates and source-drain regions, was the first run with total-dose hardness exceeding 10^6 rads (Si). The lot process parameters are given in Table 5. The hardness test data for this lot, processed with dry, undoped SiO_2 for the channel dielectric, is shown in Fig. 10. Figure 10 is a plot of total-dose hardness for inverters with inputs biased "on" during irradiation. This exhibited exceptionally good total-dose hardness, with a maximum N-transistor threshold voltage shift of 0.9 V at 10^6 rads. The N-transistor was slightly into depletion-mode operation due to the low (0.7 V) preradiation threshold voltage. At 2×10^6 rads the N-threshold voltage was again positive. This wafer lot demonstrated the feasibility of the hardened CMOS/SOS technology for small-scale integrated circuits.

TABLE 5. TRIPLE-IMPLANT PROCESS PARAMETERS (Lot S280)

- p-Epi ..... 2×10^{16} cm^{-3} (boron)
- n-Epi ..... $1\text{-}2 \times 10^{15}$ cm^{-3} (phosphorus)
- Channel Oxidation ..... 1000°C, 2 h, dry O_2, t_{ox} = 750 Å
- Polysilicon-Gate Implant Dose .. 1×10^{16} cm^{-2} boron, E = 70 keV
- Source-Drain (S-D) Implant:
  - N dose ..... 4×10^{15} cm^{-2} (phosphorus), E = 220 keV
  - P dose ..... 1×10^{15} cm^{-2} (boron), E = 70 keV
- Implant Drive, Anneal, S-D ..... 800°C, helium

D. BACK-CHANNEL LEAKAGE

When MOS devices are fabricated in SOS, the interfacial charge densities at both the $Si\text{-}SiO_2$ and the Si-sapphire interfaces must be carefully controlled. An excess of positive charge at the Si-sapphire interface will result in an n-channel device that cannot be turned off completely by the application of a negative voltage to the gate electrode; i.e., the result will be a "leaky" n-channel device. This phenomenon has been termed "back-channel" leakage.

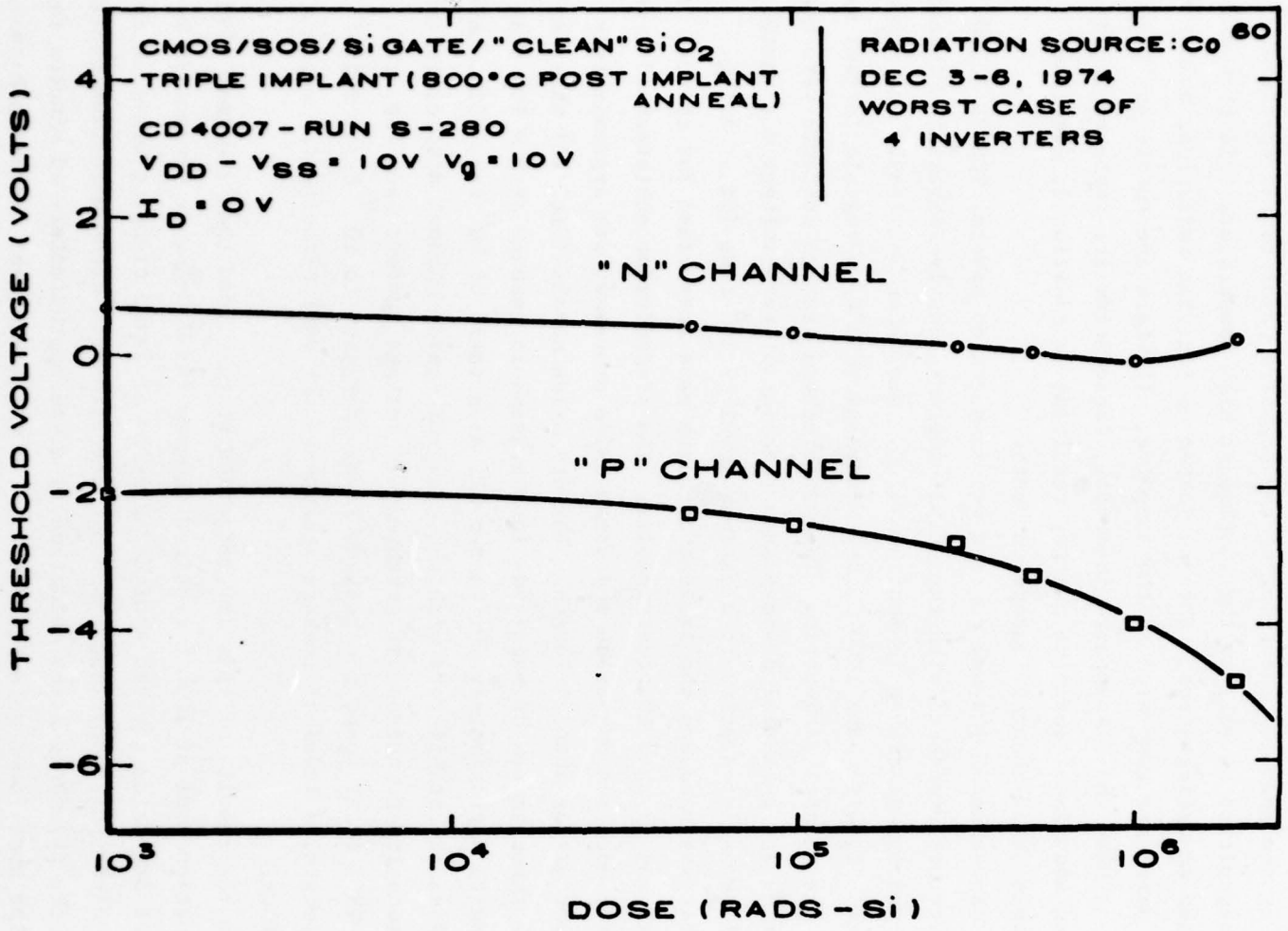

Figure 10. Radiation hardness data for lot S280.

The amount of this interfacial charge at the Si-sapphire interface can be affected by the thermal processing of the sapphire prior to the epitaxial silicon deposition as well as the subsequent high-temperature oxidation diffusions and annealing steps. When subjected to ionizing radiation, hole-electron pairs are generated in the sapphire. If there are sufficient trapping sites at or near the Si-sapphire interface, these holes are captured and give rise to an additional positive charge, resulting in additional, non-gate-controllable, back-channel leakage currents.

The back-channel leakage current was measured on several TCS071 (CD4007A type) inverters processed with the triple-implant, double-epitaxial, radiation-hardened process described in Section VII.C. One wafer lot (S539) was processed as a split lot, with both 1000°C, dry oxide and (925°C) pyrogenic (steam) oxides used for the channel dielectric. The subthreshold leakage currents were measured for n- and p-channel devices as a function of gate voltage for various levels of gamma irradiation to a maximum level of 10^6 rads (Si). A log-picoammeter was used and the leakage currents were normalized for channel length. Figures 11 and 12 show the test results. The preradiation subthreshold leakage current for both the dry-oxide and steam-oxide processes was approximately 10^{-11} A per mil of channel length. The dry oxide sample (Fig. 11) shows an increase of three orders of magnitude in subthreshold leakage at 5×10^4 rads (Si), increasing to approximately 10^{-7} A per mil at a total of 10^6 rads (Si). After irradiation, the transistors with the pyrogenic-oxide channel dielectric exhibited a much lower increase in subthreshold leakage current (see Fig. 12). At 10^6-rads (Si) total dose, the leakage level increased to 10^{-9} A per mil of channel length, a level of leakage acceptable for VLSI circuits for megarad environments.

From the results of this investigation we concluded that the long ($\sim$90 min) oxidation time at 1000°C required to grow the 750-Å-gate dielectric by the use of dry oxide created a higher density of fixed trapping sites at or near the Si-sapphire interface than did the pyrogenic steam oxidation cycle. At 925°C the pyrogenic steam oxidation time was approximately 45 minutes for growing the same 750-Å gate dielectric. In all subsequent radiation-hardened processing the pyrogenic oxidation was employed for the gate dielectric.

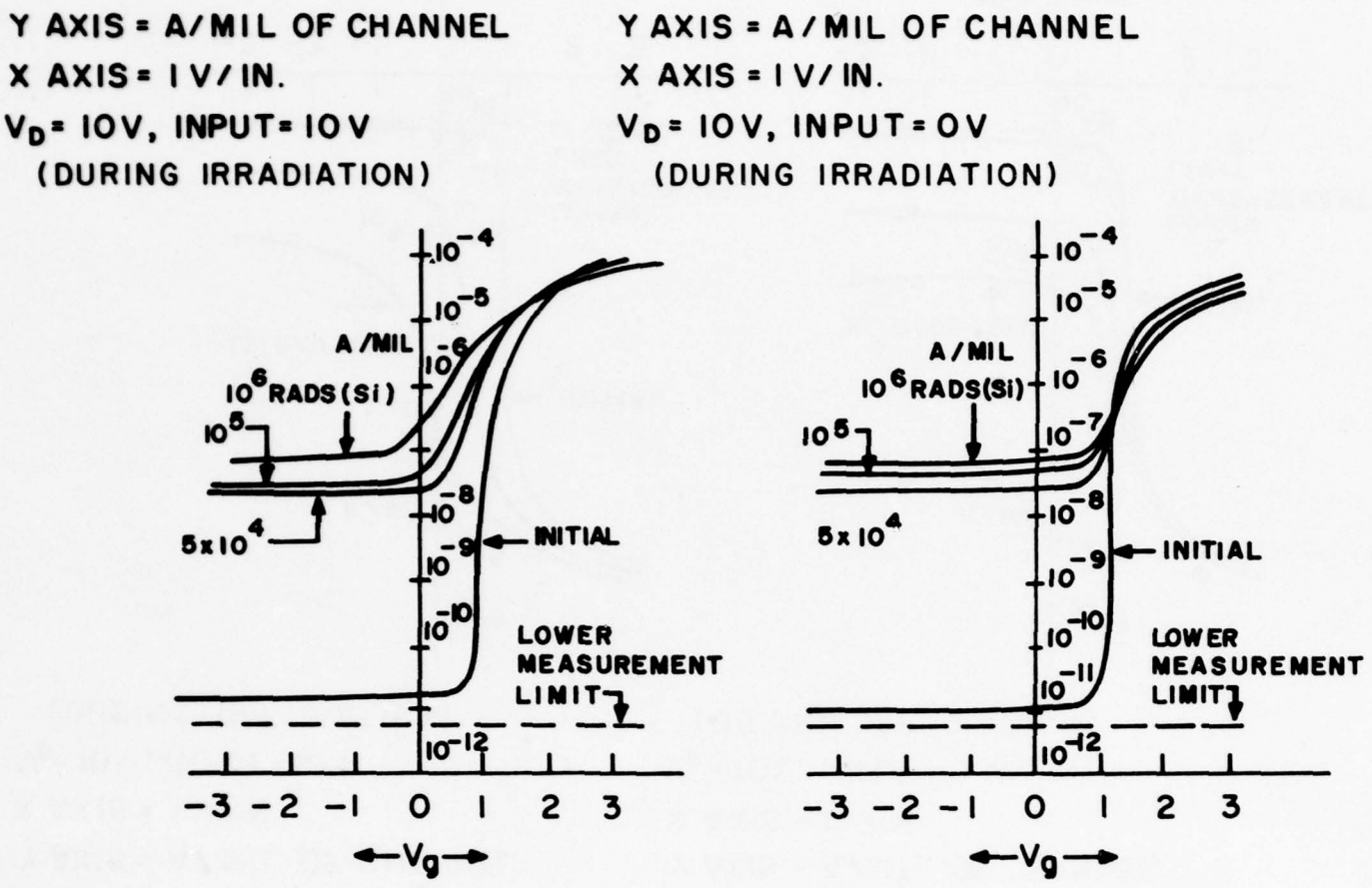

Figure 11. Subthreshold leakage vs radiation (dry oxide).

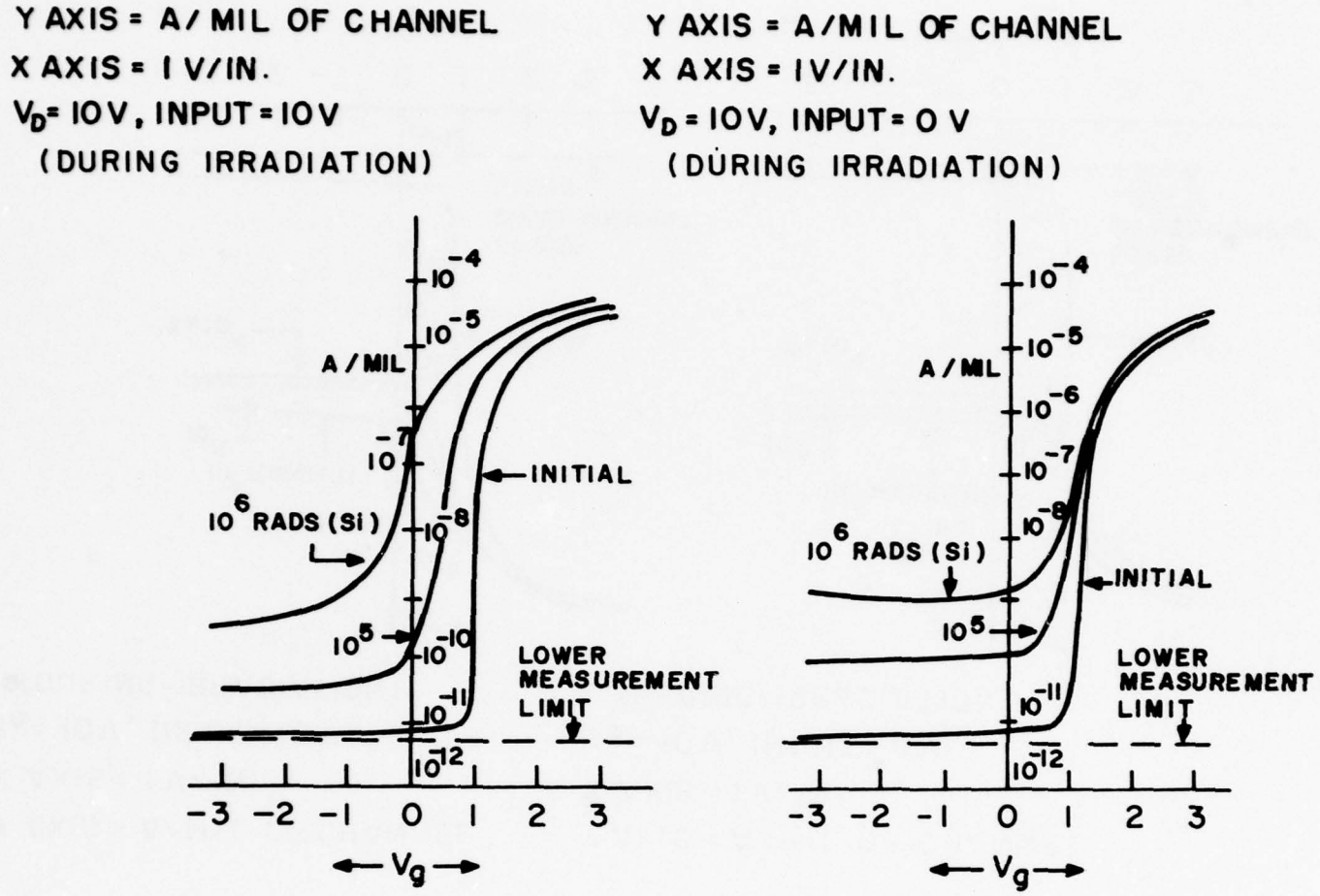

Figure 12. Subthreshold leakage vs radiation (pyrogenic oxide).

E. IN SITU-DOPED POLYSILICON

The doping of the polysilicon gate by implantation requires a heavy boron dose to get as low a sheet resistivity in the gate conductor as possible. The dopant species must also be implanted as close to the $Si-SiO_2$ interface as possible, without penetrating into the gate insulator. This requires extremely tight control of both the implant schedule and the polysilicon thickness. In practice we found that the polysilicon-gate thickness varies as much as $\pm$10% from the nominal value over a 3-in.-diam wafer. For this reason, and also to improve the economic viability of the process, an investigation of other techniques for doping the polysilicon was undertaken.

A technique for depositing boron-doped polysilicon at low temperature was developed at RCA's David Sarnoff Research Center. The polysilicon layer is deposited at 620°C by the pyrolysis of silane in a hydrogen atmosphere. The dopant gas, diborane, is introduced into an AMV-1200 reactor simultaneously with the silane mixture. The reactor capacity is eight 3-in.-diam wafers and the cycle time is approximately one hour. The flow rate of the diborane gas was chosen by experiment to achieve doped polysilicon of sufficiently low sheet resistance while retaining good etching characteristics. Typical sheet resistance is 40-60 $\Omega/\square$ after a 90-min, 850°C, drive cycle.

POS (polysilicon-oxide-silicon) capacitors were fabricated by deposition of this in situ-doped polysilicon on 750-Å pyrogenic steam oxides. These capacitors were radiation tested and subjected to 300°C CVBT tests for stability. The radiation-test data (see Fig. 13) show less than a 2.0-V shift at a 10^6-rad (Si) total dose, indicating this structure to be equivalent to implanted polysilicon-gate structures. The CVBT test data, Fig. 14, demonstrated no inherent stability problems. This method for depositing the polysilicon then was chosen to replace the boron-implanted-gate process for hardened LSI circuit fabrication.

F. IMPLANT PROCEDURES FOR HARDENED LSI ARRAYS

Ion implantation of the source/drain regions had a minimal effect on fabrication yield for the small-area TCS071 arrays processed for this contract. Yield at circuit probe was typically 50%. When a high-current ion implanter (Extrion Model 200-1000) was used for the P^+ and N^+ source-drain implant steps on large-area LSI array types, the process yields were extremely low. There

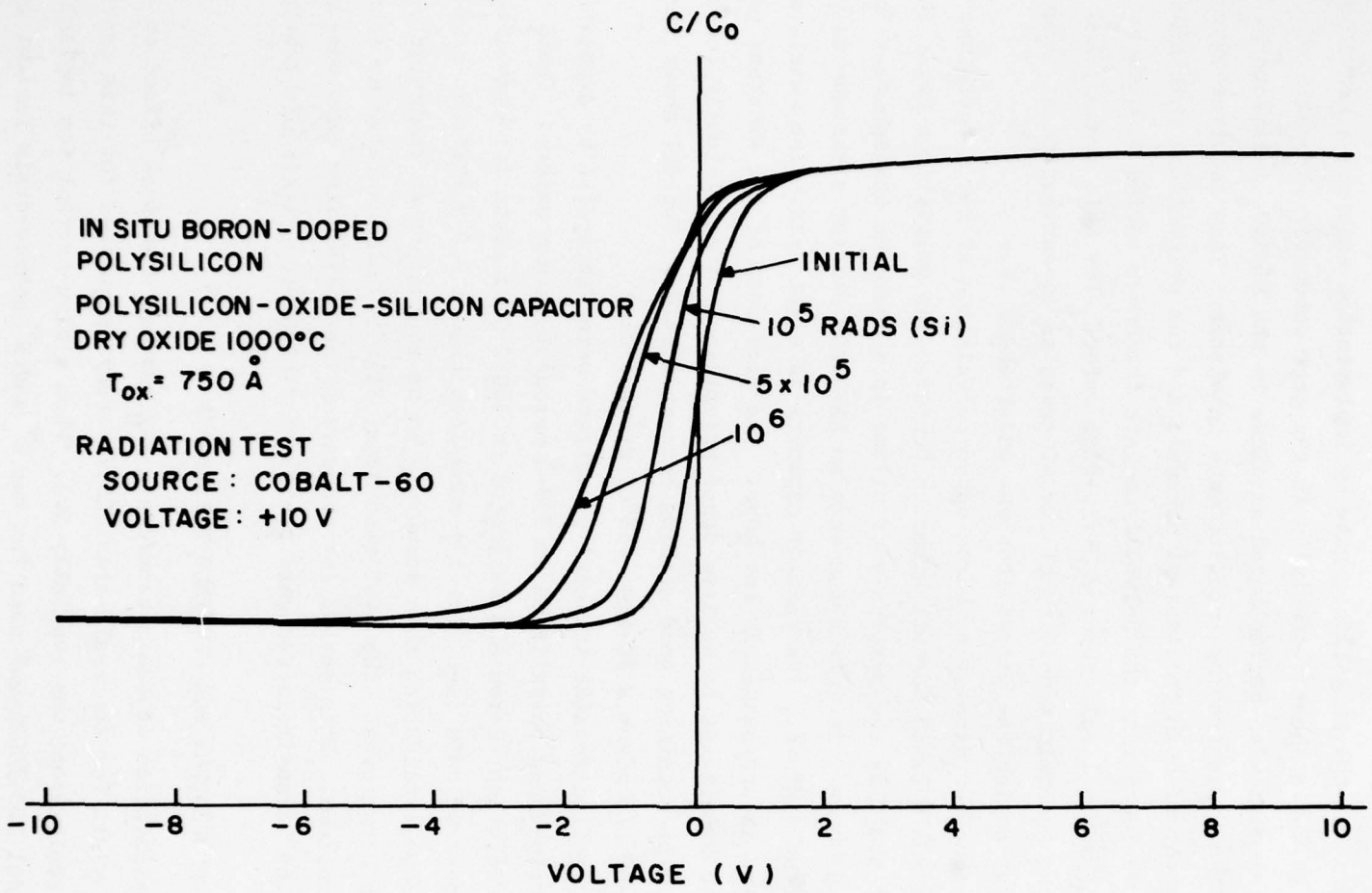

Figure 13. Radiation test data, POS capacitor.

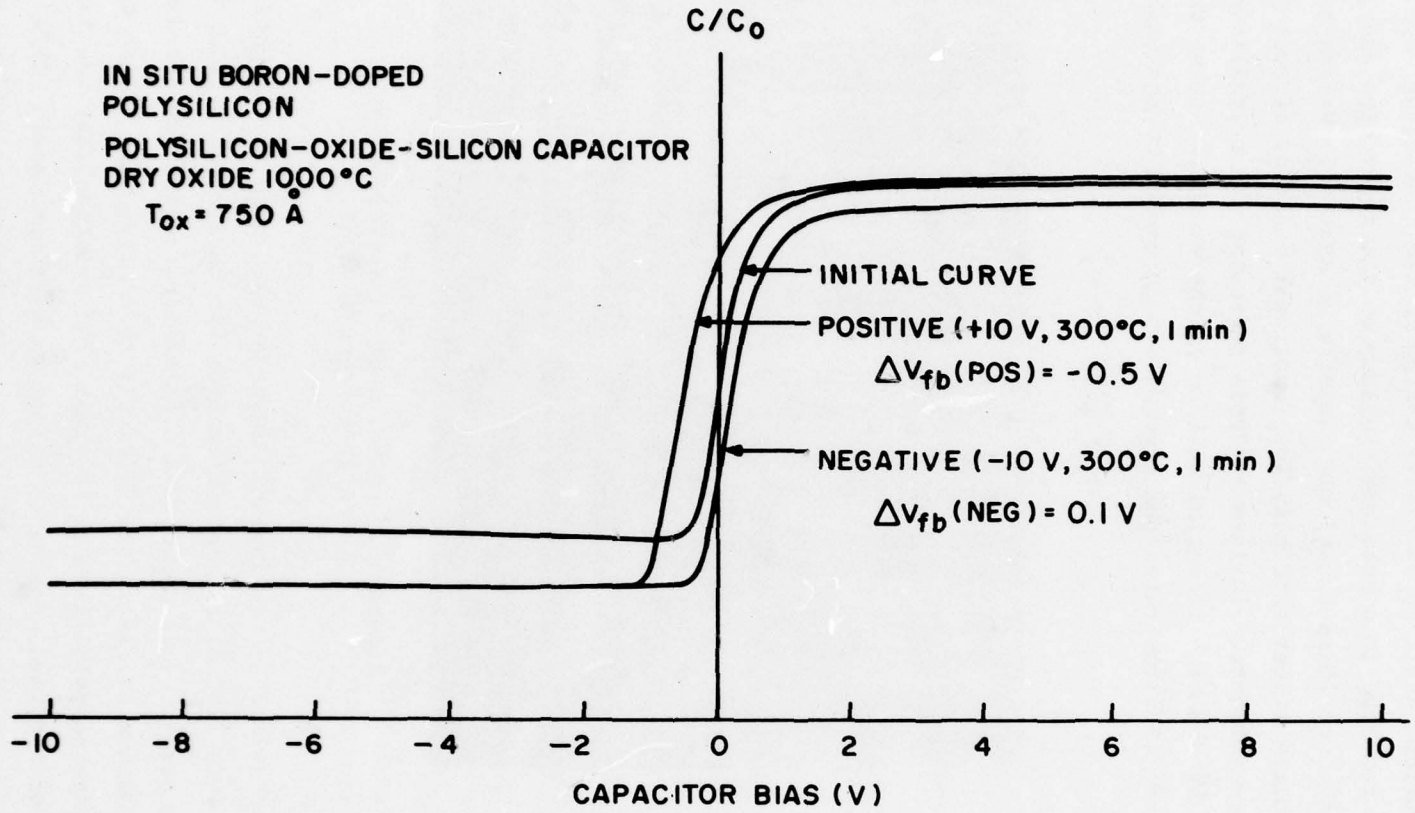

Figure 14. CVBT test data, POS capacitor.

was wafer breakage in the ion implanter. Investigation revealed that the high ion-beam current built up excessive charge on the insulating sapphire surface. The charge resulted in a potential buildup on the wafer high enough (>18,0000 V) to cause arc-over; this caused the sapphire to shatter. Wafers that did not break exhibited either extremely low functional yield at circuit probe, or high-leakage currents. Failure analysis indicated the polysilicon gates had been blown by the high potential buildup on the sapphire during the implant step. Figure 15 illustrates the type of damage caused by the high-current implanter.

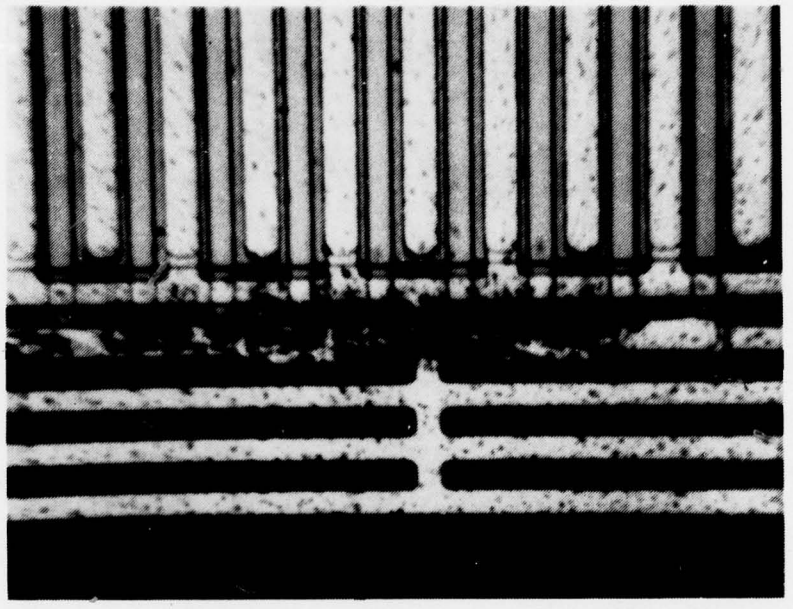

Figure 15. Polysilicon damage caused by high-current implant.

Two solutions to the implant damage problem were investigated. One was to deposit a thin (200 Å) aluminum film over the entire wafer prior to the implant processing steps. This conductive film eliminated the implant-damage problem, but the aluminum thickness was difficult to control with either the filament- or induction-heated metallization systems. The solution that was finally adopted consisted of modified masking to define an aluminum layer. This layer (≈10,000-Å thick) served as the implant barrier for the implant as well as the conductive

layer for bleeding off excessive charge from the wafer surface during the implant step. The designs for the N^+ and P^+ implant masks were complementary, so that only one additional mask had to be generated for both implant steps. The solution to masking problems is illustrated in Fig. 16(b).

G. HARDENED CMOS/SOS LSI CIRCUIT FABRICATION

1. Introduction

Under a separate contract (NRL N00014-75-C-0709) RCA's Advanced Technology Laboratories designed and evaluated a multiport silicon-gate, CMOS/SOS standard-cell family designed for maximum transient upset and total-dose hardness. To evaluate the cell family a test chip (TCS059) and arithmetic logic unit (ALU) (TCS069) integrated circuits were designed and fabricated. The radiation-hard cells were designed to compensate for both total-dose and transient-radiation effects. For total-dose effects the following were considered: (1) changes in threshold voltage and mobility, (2) the irradiation bias dependence of n- and p-channel transistors, and (3) increased subthreshold leakage of n-channel transistors. Improved transient upset performance from both junction and sapphire photocurrents was obtained by (1) minimization of channel length and gate-oxide thickness, (2) high noise margins, (3) utilization of optimum n- and p-channel width ratios, (4) limitation on fan-in, and (5) redesign of certain logic functions. A microphotograph of the TCS059 test chip is shown in Fig. 17. Figure 18 shows the TCS069 ALU chip.

2. Processing

The TCS059 and TCS069 arrays were fabricated by the 1000°C dry and pyrogenic channel-oxidation procedures with ion implanting of sources, drains, and silicon gates, followed by an 850°C implant activation and anneal step. The channel-oxide thickness ranged from 700 to 850 Å. Carrier concentrations in the n- and p-epitaxial layers were specified to provide initial $V_{TH_N} \sim 1.5$-2.0 V and $V_{THp} \sim 1.0$-1.5 V. An rf-heated source was used for metal deposition.

3. Electrical Evaluation of TCS059

Electrical evaluation indicated functional performance of all cells with noise immunity ranging from 3.5 to 5.0 V. Dynamic evaluation indicated cell

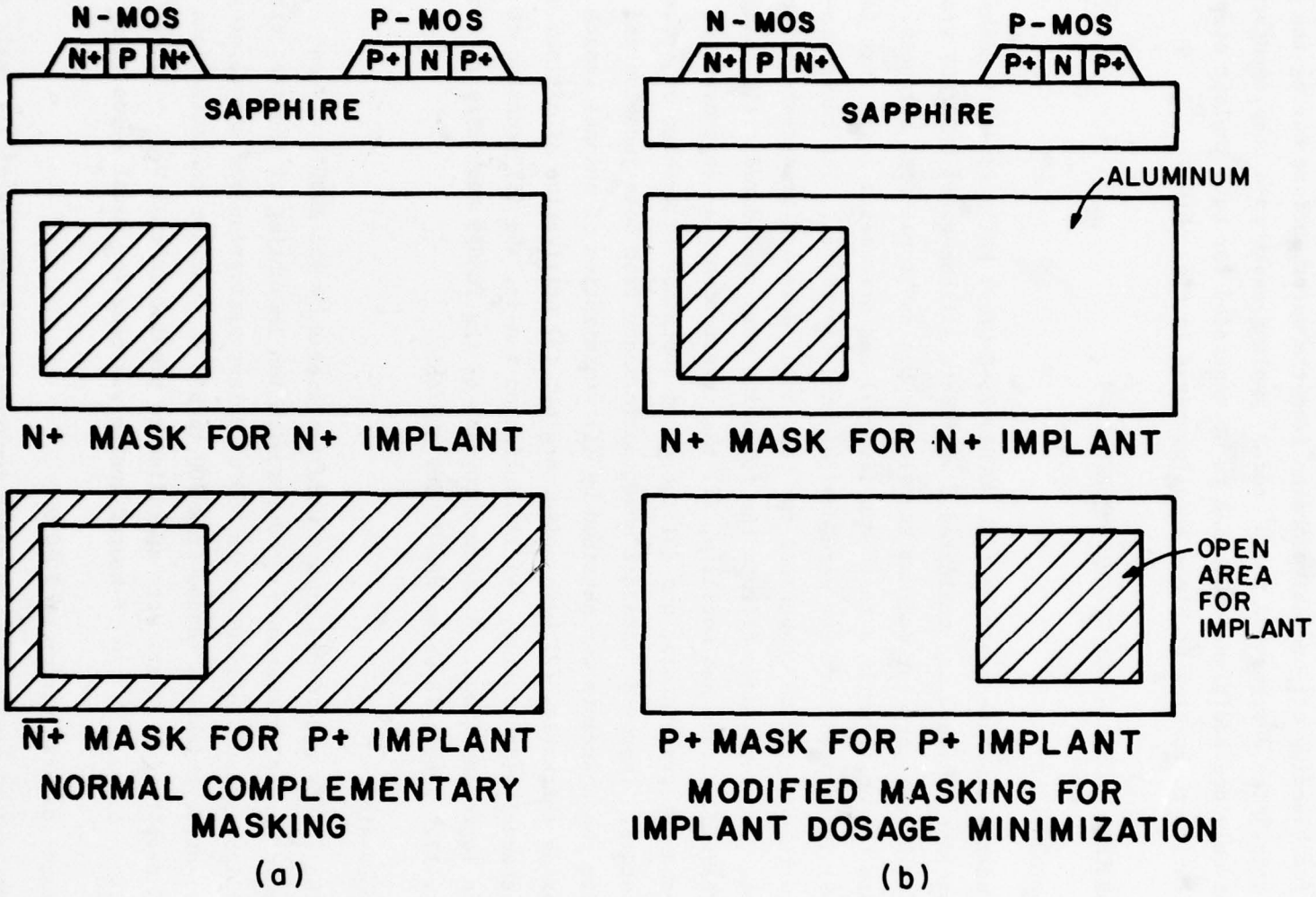

Figure 16. Masking solution for N^+ and P^+.

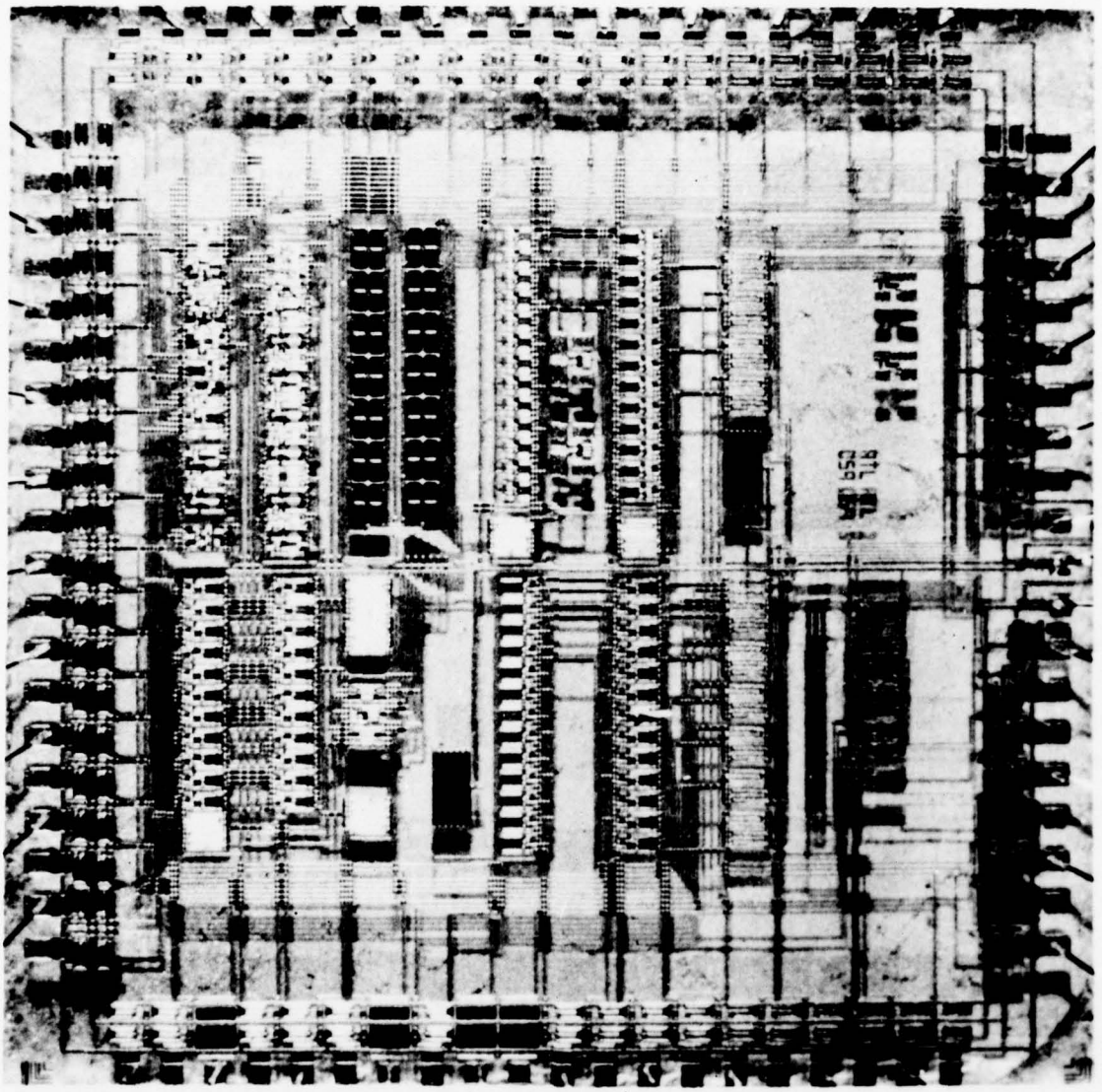

Figure 17. Photomicrograph of TCS059 test chip employed for standard-cell evaluations.

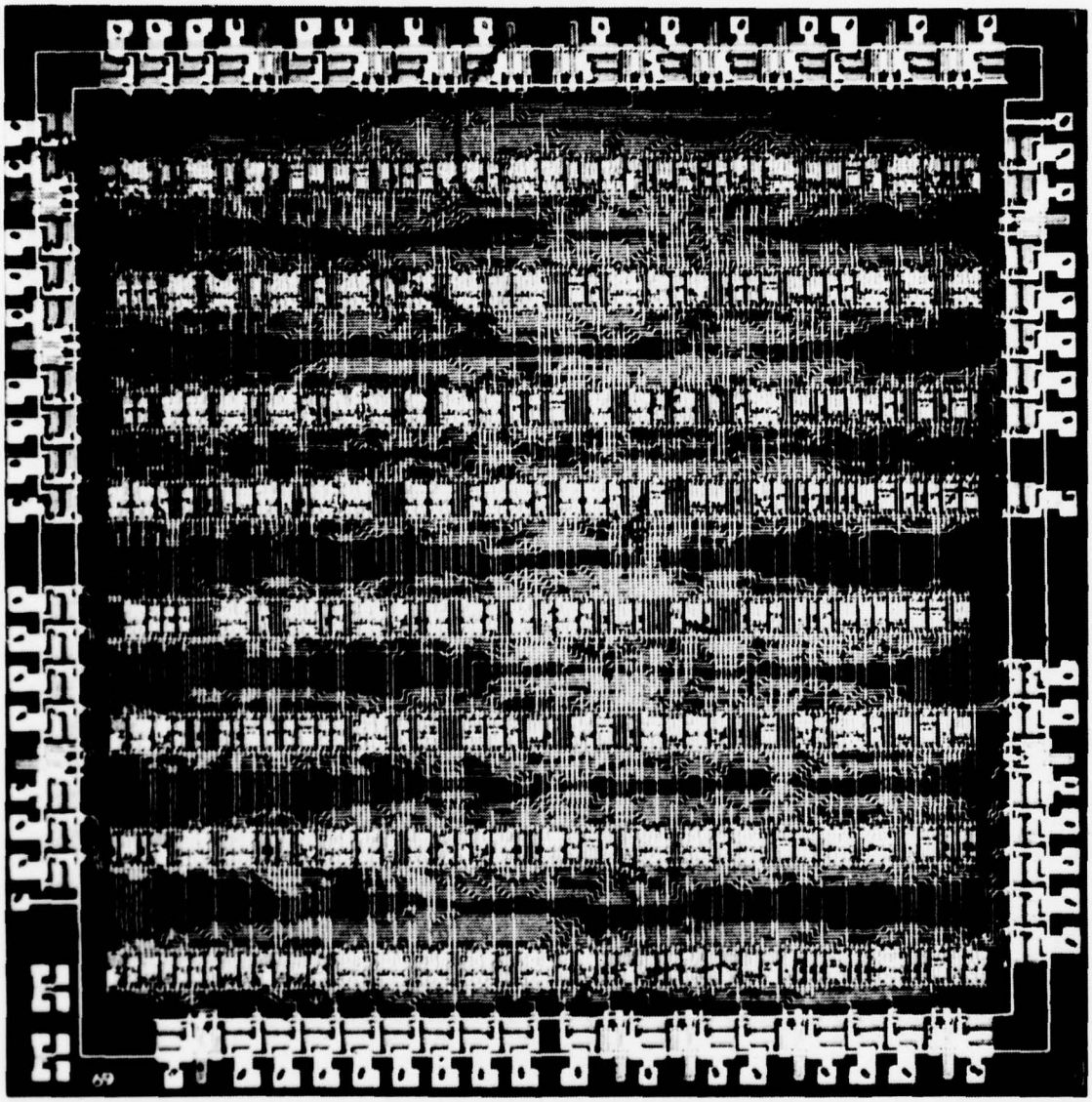

Figure 18. Photomicrograph of radiation-hard TCS069 ALU chip.

speeds about a factor of 2 slower than predicted. Analysis indicated that reduced speed resulted from (1) lower mobility obtained by use of the triple-implant ($3I^2$) process, (2) larger channel length due to mask tolerances and minimal lateral diffusion of the implanted sources and drains, and (3) a slight underetching of the polysilicon gates during processing. Optical measurements indicated an effective channel length near 0.3 mil. Saturation currents for the n- and p-channel transistors were 1 mA/mil and 0.6 mA/mil, respectively, compared with the expected 2 mA/mil and 1.0 mA/mil saturation currents. As a result of the added capacitance of the substrate connection, the radiation-hard cells, compared with conventional cells, exhibited a speed reduction of approximately 20%.

4. Transient Upset Testing of TCS059

The test chip was irradiated at Naval Research Laboratory by use of the 40-MeV LINAC with 60-ns to 1-μs electron pulses. The electron-pulse shape was monitored by means of a PIN diode, while the total dose for each pulse was measured with an array of four 1/8-in. TLD dosimeters attached to the IC case. The outputs from a divide-by-eight counter and a static flip-flop were monitored on two dual-beam Tektronix 556 oscilloscopes. In additional tests, in which lead shields and dummy devices were used to evaluate possible spurious signals, five samples from two wafers were exposed to radiation.

The transient upset level for the sequential logic elements was found to be greater than 10^{11} rads (Si) per second. The upset level for the flip-flop and counter were similar (within 30% of 10^{11} rads/s) as was the upset level from either the "zero" or the "one" state. No significant decrease in the upset level was noted from transient annealing, total-dose effects at the 1-μs pulse widths (maximum obtainable with NRL LINAC), or effects at dose levels of 50-80 krads (Si) per pulse.

5. Arithmetic Logic Array (TCS069)

The ALU chip size is 5.7 mm x 5.7 mm (223 mils x 223 mils) and contains 1818 transistors. Electrical evaluation of radiation-hard processed arrays indicated an 8-bit add time of 100 ns and a 32-bit add time of 200 ns. These measurements indicate an average cell delay of 6.5 ns. The measured worst-case delay path was 9.5 ns.

Transient-upset measurements agreed with TCS059 test-chip results, indicating flip-flop upset for short pulses between 1 and 2 x 10^{11} rads (Si) per second. At these irradiation rates the total chip-current pulse is about 1 A (peak). The current response essentially follows the irradiation pulse.

Hybrid-oxide units with high initial leakage (1-10 mA) were produced. Leakage was caused by low-breakdown devices. ALUs from this group were irradiated, and complete functional performance was verified to greater than 3 x 10^{5} rads (Si). A speed loss of less than 5% was noted at this dose level. The chip current increased from preirradiation values of 0.5-4 mA (leakage depends on input state) to a range of 1-6 mA after irradiation. Subsequent lots of this device had leakage levels of 200 μA, but were not radiation tested. Cobalt-60 irradiation test data for the test inverter on the TCS069 wafer are shown in Fig. 19.

A paper [4] summarizing the aluminum-gate and silicon-gate radiation-hardened process development was presented at the 1976 IEEE Nuclear and Radiation Effects Conference.

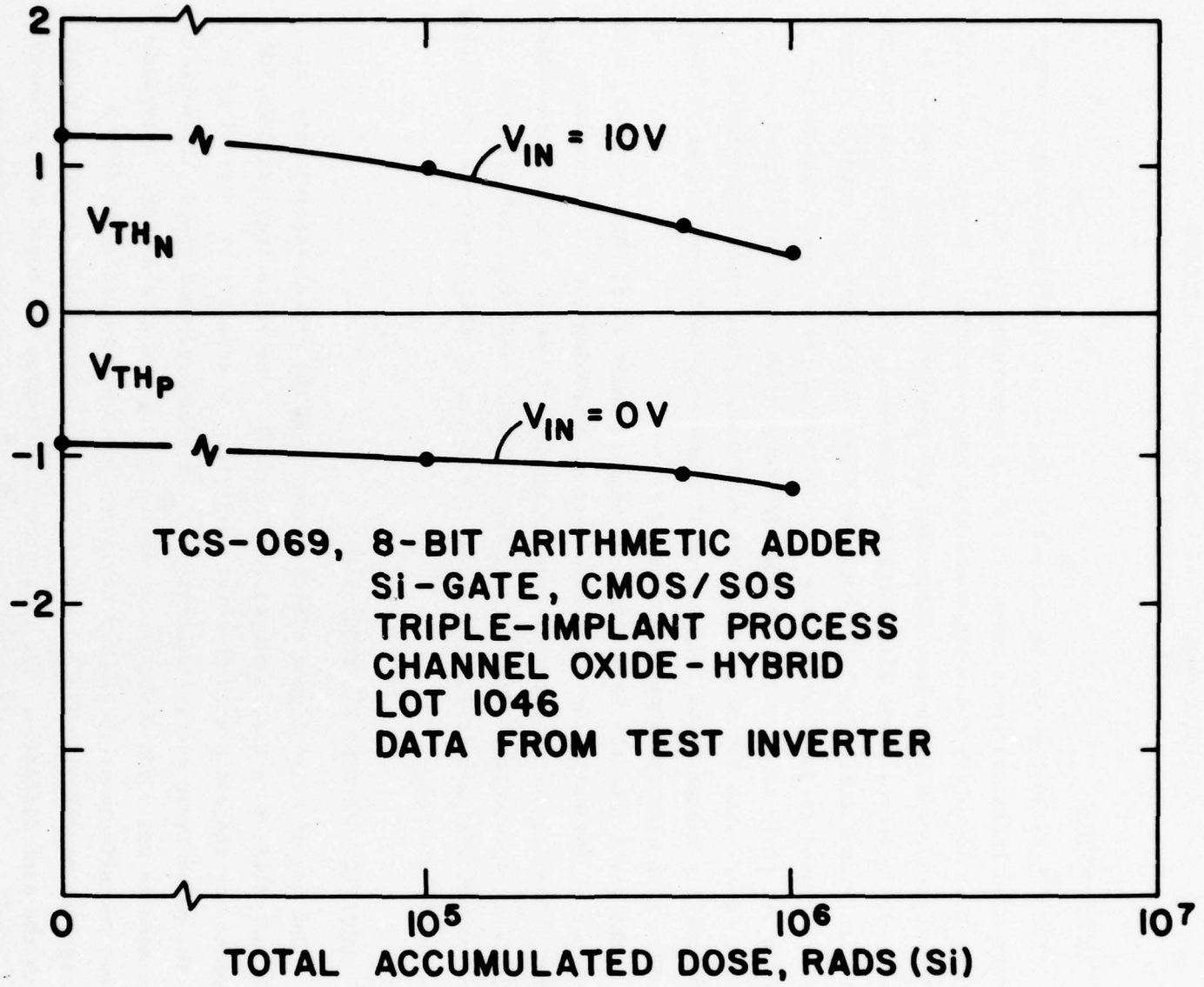

Figure 19. TCS069 radiation test data.

SECTION VIII

RADIATION-HARD PROCESS DEVELOPMENT FOR CLOSED CMOS LOGIC (C^2L)

A. INTRODUCTION

The C^2L technology was introduced by RCA to provide higher-density CMOS arrays with increased speed capability while preserving the inherent CMOS advantages of low power consumption and high noise-immunity. In this technology, self-aligned polysilicon-gate structures and completely enclosed drain areas are used. A source plane eliminates the individual source connections required for each transistor. The fully enclosed source/drain geometry totally eliminates the need to guardband, since no uncontrolled current path between the source and drain can occur. The C^2L structure, combining self-aligned silicon gates with low parasitic drain capacitance, has transistors having a considerably higher speed, higher mutual transconductance, and higher packing density than aluminum-gate CMOS arrays.

The Naval Research Laboratory, as part of Phase IV of this contract, added the task of investigating the feasibility of hardening the C^2L technology. The array chosen to demonstrate the process capability was the RCA-designed CDP1802 COSMAC microprocessor. This array is an LSI CMOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element.

B. RADIATION-HARDENED C^2L PROCESSING

The use of self-aligned silicon gates made the processing sequence for C^2L very similar to that employed for CMOS/SOS. The radiation-hard CMOS/SOS process was therefore used wherever possible. Because of the critical effect of the polysilicon sheet resistivity on the microprocessor speed, the decision was made to use a 950°C phosphorus diffusion for the gate doping. A typical sheet resistivity of 15 Ω/□ was achieved with a 26-min diffusion from a phosphorus oxychloride ($POCl_3$) source. The N^+ source-drain region was doped with the same diffusion. The P^+ source-drain region was doped with a 70-keV boron (B^+) dose (3×10^{15} cm^{-2}). The channel-oxide thickness, grown with dry oxide and quenched, was 700 Å. Metallization was 1% silicon-aluminum,

deposited by induction-heating. Proper control of the Si-Al composition was essential to prevent alloying of the aluminum into the shallow junction source/drain regions. Excessive silicon percentage resulted in poor wire-bonding. The principal features of the process are summarized in Table 6.

TABLE 6. C^2L RADIATION-HARDENED PROCESS SUMMARY

• Well Implant	Boron, 100 keV; dose, 4×10^{13} cm^{-2}
• Channel Oxidation	Dry O_2, 700 Å, no anneal, quenched
• Polysilicon	Deposited intrinsic, 5000 Å
• P^+ Source-Drain Implant	Boron, 70 keV; B^+ dose, 3×10^{15} cm^{-2}
• N^+ Source-Drain plus Gate Doping	950°C, $POCl_3$, 26 min
• Field Oxide Densification	875°C, 30 min
• Metallization	12,000 Å (1% Si-doped Al)
• Alloy	450°C, 30 min, N_2

Several runs of the CDP1802 microprocessor were fabricated by the process described. The well-implant schedule increased the nominal N-transistor threshold voltage to 1.7 V for zero drain current. This initial threshold voltage level was sufficiently high to prevent depletion-mode operation to beyond 10^6 rads (Si) total dose.

C. TEST RESULTS

In preliminary radiation testing performed at RCA, the RCA Microkit was used to exercise the microprocessor. An external clock, a 300-kHz square wave, was used because of the long cable harness required for inserting the array into the cobalt-60 radiation test chamber. Chip-leakage current was continuously monitored while the device was being irradiated. The current increased from about 20 μA (preradiation) to 150 μA at 10^6-rads (SI) total dose. The failure mode was a soft failure, caused by a continuous increase in negative shift of the p-channel transistor-threshold voltage with increasing dose. At 5×10^5 rads, the arrays would not pass the 5-V functional test, but did pass 7-V functional tests. Operational speed also decreased because of the increasingly negative P-transistor-threshold voltage. Packaged CDP1802 arrays were shipped to Naval Research Laboratory for more extensive radiation tests [5].

SECTION IX

CONCLUSIONS

This section summarizes the results of the studies conducted under this contract.

A. CHANNEL-OXIDATION AND ANNEAL STUDIES

Dry O_2 grown, 1000°C, undoped oxides, without anneal but quenched, resulted in the maximum total-dose radiation hardness for the aluminum-gate technology. This oxidation technique does cause increased back-channel leakage current on CMOS/SOS arrays.

Lower-temperature steam oxides (850-925°C), with or without HCl, are suitable for Mrad-hard LSI array fabrication, provided the postoxidation processing temperatures do not exceed the channel-oxidation temperature.

B. ALUMINUM EVAPORATION

The electron-beam melting technique for the deposition of aluminum causes increased P-transistor-threshold-voltage shifts with radiation. Filament heating or rf heating of aluminum should be used for radiation-hardened circuit fabrication.

C. BULK CMOS (ALUMINUM-GATE) RADIATION-HARD PROCESSING

A reproducible, radiation-hardened process was defined by the use of 1000°C, dry, undoped, quenched channel oxidation and induction-heated metallization. Preradiation N-transistor-threshold voltage was adjusted by the well-implant schedule for a range of 1.5 to 2.0 V. The optimum channel-oxide thickness for this process is 700-800 Å. The longer oxidation time required for the dry (rather than steam) oxidation increases lateral diffusion. Source/drain spacing must be increased to provide adequate source/drain breakdown voltage, when 1000°C oxidation is performed.

D. BULK CMOS (SILICON-GATE) RADIATION-HARD PROCESSING

RCA's commercial C^2L process was modified for increased total-dose radiation hardness. The feasibility of producing Mrad-hard CDP1802 microprocessors was demonstrated. The principal process modifications were: Use of 950°C

diffusion for the polysilicon gates and the N^+ source drains, ion implantation of the P^+ source drains, and 850°C drive-in and anneal temperature. The preferred channel-oxidation technique was pyrogenic oxide.

E. SILICON-GATE CMOS/SOS PROCESSING

A triple-implant process was developed for fabricating radiation-hardened CMOS/SOS LSI arrays. A technique for implanting the source drains and polysilicon gates using high-current implant equipment was developed. Additional study is required to develop more reproducible techniques for doping the polysilicon gate.

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